Assignment 3

1. Consider the following source code:

```c
int main() {
    int a = 5;
    int b = 6;
    int c = a + b;
    printf("The sum is %d\n", c);
    return 0;
}
```

What is the output of this program?

2. A computer has a memory map as follows:

```
 00000 - 0009F: 1K RAM
 00100 - 0017F: 1K ROM
 00180 - 001FF: 256-byte programmable read-only memory
 00200 - 002FF: 512-byte programmable RAM
 00300 - 003FF: 256-byte programmable ROM
```

What are the boundaries of the ROM and RAM areas?

3. The instruction set of a computer includes the following instruction formats:

- Add: `ADD Rn, Rm, R3`
- Subtract: `SUB Rn, Rm, R3`
- Multiply: `MUL Rn, Rm, R3`
- Divide: `DIV Rn, Rm, R3`
- Load: `LDR Rn, [Rm]`
- Store: `STR Rn, [Rm]`

What is the number of registers in the instruction set?

4. The following diagram depicts a simple CPU architecture:

![CPU Architecture Diagram](image)

Describe the function of each component in the diagram.

5. The instruction `ADD R1, [R2]` is executed on a processor with a Harvard architecture. An instruction cache and a data cache are implemented. How would this instruction be executed?

6. In the Harvard architecture, the instruction cache contains a program counter (PC) and the instruction memory, while the data cache contains the data memory. What is the advantage of this architecture?

7. A processor with a Harvard architecture has a program counter (PC) and an instruction memory. The program counter is incremented by the length of the instruction. Which of the following instructions has the longest execution time?

- `ADD R1, R2`
- `LDR R1, [R2]`
- `STR R1, [R2]`

8. The instruction `LDR R1, [R2]` is executed on a processor with a Harvard architecture. The instruction cache contains the program counter (PC) and the instruction memory, while the data cache contains the data memory. What is the sequence of events when this instruction is executed?

- Fetch the instruction from the instruction cache
- Fetch the data from the data cache
- Execute the instruction
- Update the program counter

9. The following diagram depicts a simple CPU architecture with an instruction cache and a data cache.

```
  +-----------------+  +-----------------+
  | Instruction PC  |  | Data Memory      |
  +-----------------+  +-----------------+
               /                          |
              /                            |
             /                             |
            /                             |
           /                             |
          /                             |
         /                             |
        /                             |
       /                             |
      /                             |
     /                             |
    /                             |
   /                             |
  +-----------------+  +-----------------+
  | Instruction PC  |  | Data Memory      |
  +-----------------+  +-----------------+
```

Describe the sequence of events when the program counter is incremented.

10. In the Harvard architecture, the instruction cache contains a program counter (PC) and the instruction memory, while the data cache contains the data memory. Which of the following instructions has the longest execution time?

- `ADD R1, R2`
- `LDR R1, [R2]`
- `STR R1, [R2]`

11. The instruction `LDR R1, [R2]` is executed on a processor with a Harvard architecture. The instruction cache contains the program counter (PC) and the instruction memory, while the data cache contains the data memory. What is the sequence of events when this instruction is executed?

- Fetch the instruction from the instruction cache
- Fetch the data from the data cache
- Execute the instruction
- Update the program counter

12. The following diagram depicts a simple CPU architecture with an instruction cache and a data cache.

```
  +-----------------+  +-----------------+
  | Instruction PC  |  | Data Memory      |
  +-----------------+  +-----------------+
               /                          |
              /                            |
             /                             |
            /                             |
           /                             |
          /                             |
         /                             |
        /                             |
       /                             |
      /                             |
     /                             |
   +-----------------+  +-----------------+
   | Instruction PC  |  | Data Memory      |
   +-----------------+  +-----------------+
```

Describe the sequence of events when the program counter is incremented.