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Courses » Computer Organization and Architecture

Announcements **Course** Forum Progress Mentor

Unit 9 - Week 8

Course outline

How to access the portal

Week 1

Week 2

Week 3

Week 4

Week 5

Week 6

Week 7

Week 8

- Lecture 25 - Structural Hazard, Architectural Enhancements
- Lecture 26 - Lab 3: Shared Memory Architectures
- Lecture 27 (Part 1) - Locality of Reference, Demand paging
- Lecture 27 (Part 2) - Page Replacement Algorithm
- Lecture 28 - Multilevel Paging, Translational Lookaside Buffer
- Quiz : Week 8 Assignment
- Feedback for week 8

Week 8 Assignment

Assignment Week 8

1) Structural hazards happen due to

1 point

- too many instructions in pipeline
- un-executable instructions in pipeline
- enough execution units not being available
- Error in an execution unit

Accepted Answers:

enough execution units not being available

2) Amdahl's law gives a measure of

1 point

- Time
- Area
- Power
- Speedup

Accepted Answers:

Speedup

3) Which of the following is virtual memory?

1 point

- RAM
- Cache
- Hard Disk
- None of the above

Accepted Answers:

None of the above

4) Address Translator is required to

1 point

- Convert from Physical Memory Address to Virtual Memory Address
- Convert from Virtual Memory Address to Physical Memory Address
- Convert Page Number to Page Frame Number

Assignment 8
Solutions

Week 9

Week 10

Week 11

Week 12

None of the Above

Accepted Answers:

Convert from Virtual Memory Address to Physical Memory Address

5) The Memory Translation Unit gives a page fault when

1 point

- A Physical Address is not present in the Physical Memory
- A Logical Address is not present in the Logical Memory
- A Physical Address is not present in the Virtual Memory
- A Logical Address is not present in the physical memory

Accepted Answers:

A Logical Address is not present in the physical memory

6) A page fault handler is managed by

1 point

- Programming Language
- Process
- Operating System
- Memory Translation Unit

Accepted Answers:

Operating System

7) Spatial Locality of Reference is based upon

1 point

- The probability of the same instruction being accessed in small timing intervals
- The probability of same data being fetched in subsequent instructions
- The probability of data from same page being accessed in subsequent instructions
- None of the Above

Accepted Answers:

The probability of data from same page being accessed in subsequent instructions

8) The page translation table will be

1 point

- always in logical memory only
- In physical memory but not in logical memory
- always in physical memory
- None of the above

Accepted Answers:

always in physical memory

9) The valid bit from a page address is set to 1 when

1 point

- The page is loaded into the main memory
- The page is present in the logical memory
- The page is present in the disk memory
- None of the above

Accepted Answers:

The page is loaded into the main memory

10) The dirty bit in the page address is set to 1 when

1 point

- A page is removed from the main memory
- When a modification has been made to the loaded page
- When the page is no longer valid
- When the page is not available for use

Accepted Answers:

When a modification has been made to the loaded page

11) Multi-level paging enables

1 point

- storing more pages in main memory
- dynamically shrinking and growing page tables
- Faster access
- None of the above

Accepted Answers:

dynamically shrinking and growing page tables

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End

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