



Unit 6 - Week 5

Course outline

How to access the portal

Week 1

Week 2

Week 3

Week 4

Week 5

Lecture 12 - Orthogonal ISA, C Constructs Mapping, Addressing Modes

Lecture 13 - Atomic and Predicated Instructions

Lecture 14 - Atomic and Predicated Instructions (Contd.)

Lecture 15 - General Purpose Registers

Lecture 16 - Expanding opcodes

Quiz : Week 5 Assignment

Feedback for week 5

Week 5 Assignment Solutions

Week 6

Week 7

Week 5 Assignment

1) Select the true statement

1 point

- In the Load-Store architecture, all instructions use memory
- In the Load-Store architecture, instructions use minimal access to memory
- In the Load-Store architecture, only load and store access memory
- In the Load-Store architecture, every instruction works using registers

Accepted Answers:

In the Load-Store architecture, only load and store access memory

2) Choose the correct formula for Effective Address calculation

1 point

- $Base + (Size * Scale) + Displacement$
- $(Base + Size) * Scale + Displacement$
- $Base + Size * (Scale + Displacement)$
- $(Base + Size) * (Scale + Displacement)$

Accepted Answers:

*$Base + (Size * Scale) + Displacement$*

3) TestandSet(V) should be a

1 point

- predicate instruction
- atomic instruction

Accepted Answers:

atomic instruction

4) The main need for the TestandSet(V) instruction is

1 point

- Process switching
- Task Switching
- Process Synchronization
- Cache management

Week 8

Week 9

Week 10

Week 11

Week 12

Accepted Answers:

Process Synchronization

5) Atomicity of the TestandSet(V) is ensured by

1 point

- Software
- Programming Language
- Compiler
- Hardware

Accepted Answers:

Hardware

6) CMOV is a predicated instruction because

1 point

- It takes less memory
- It runs only when a condition is satisfied
- It is an atomic instruction
- It is an optional instruction

Accepted Answers:

It runs only when a condition is satisfied

7) RISC Architectures are Load-Store Architectures because of

1 point

- Fixed-Instruction Length
- Easiness for compiler
- Less number of instructions
- Large number of instructions

Accepted Answers:

Fixed-Instruction Length

8) Maximum clique in a register graph is an indicator of

1 point

- Possibility of deadlock
- Number of registers needed
- Size of the program
- Size of cache

Accepted Answers:

Number of registers needed

9) Register Spilling happens when

1 point

- There are too many registers
- There are not enough registers
- The data is larger than the register size
- There is not enough data to put in memory

Accepted Answers:

There are not enough registers

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End

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