Week 3 Assignment

1) The addressing modes involved in the following instruction are
   MOV EAX, 0x10
   - Register, Register
   - Register, Memory
   - Register, Immediate
   - Immediate, Memory

   **Accepted Answers:**
   Register, Immediate

2) What does the following instruction result in?
   DIV EAX
   - Compiler Error
   - Syntax Error
   - Divides EAX by 1
   - Divides EAX by EAX

   **Accepted Answers:**
   Divides EAX by EAX

3) The remainder of the DIV operation is stored in which of the following registers?

   **Accepted Answers:**
   EDX

4) Which of the following characterizes the memory in x86 architecture?
   - bit-addressible
   - byte-addressible
5) Which of the following characterizes the x86 architecture?

- Simple Instruction Set Architecture
- Reduced Instruction Set Architecture
- Extended Instruction Set Architecture
- Complex Instruction Set Architecture

Accepted Answers:
- Complex Instruction Set Architecture

6) PF, the parity flag checks for which of these?

- If number of 1's in the bit is even
- If the number of 1's is greater than number of 0's
- If all the bits are 0
- If all the bits are 1

Accepted Answers:
- If number of 1's in the bit is even

7) ADD AL, [0x1000] is a

- 4-bit instruction
- 8-bit instruction
- 16-bit instruction
- 32-bit instruction

Accepted Answers:
- 8-bit instruction

8) Which of the following is the correct definition of accuracy?

- How is the measured value to the true value?
- How close are results from different experiments?

Accepted Answers:
- How is the measured value to the true value?

9) In 32-bit IEEE 754 floating point format, the exponents are stored in which of the following formats?

- decimal
- excess-127
- excess-64
- exponent as integer

Accepted Answers:
What kind of processor is x86?

- RISC
- CISC
- DISC
- None of the above

Accepted Answers:
CISC