Week 12 Assignment

Assignment Week 12

1) A multi-processor system which at any point of time doesn’t need to have multiple processors accessing the same memory location is called 1 point

- Exclusive Read Exclusive Write PRAM model
- Concurrent Read Inclusive Write PRAM model
- Concurrent Read Concurrent Write PRAM model
- None of the above

**Accepted Answers:**

*Exclusive Read Exclusive Write PRAM model*

2) There is need to ensure synchronization in which of these models 1 point

- EREW
- CREW
- CRCW
- All of the above

**Accepted Answers:**

*CRCW*

3) In the case of PRAM, a barrier achieves which of the following 1 point

- Processes crosses the barrier as soon as it reaches
- Processes stop execution at the barrier
- Each process waits until another process stops at the barrier
- Each process waits until all the processes complete the execution.

**Accepted Answers:**

*Each process waits until all the processes complete the execution.*

4) Which of these is the characteristic of an optimal algorithm 1 point

- No. of processors * Time < Complexity of best known sequential algorithm
- No. of processors * Time <= Complexity of best known sequential algorithm
- No. of processors * Time = Complexity of best known sequential algorithm

**Accepted Answers:**

*No. of processors * Time < Complexity of best known sequential algorithm*
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No. of processors * Time = Complexity of best known sequential algorithm

5) Consider the following scenario. Core P1 holds an address A1 in exclusive state and it is connected to two other processors P2 and P3 through a common bus. There won't be any communication on the bus when

- P1 writes to A1 in P2
- P3 writes to A1 in P3
- P3 writes to A1 in P1
- P1 writes to A1 in P1

Accepted Answers:
P1 writes to A1 in P1

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