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Courses » Computer Organization and Architecture

Announcements **Course** Forum Progress Mentor

# Unit 13 - Week 12

## Course outline

### How to access the portal

### Week 1

### Week 2

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### Week 12

- Lecture 38 (Part 2) - Lab 4 : Task Switching ( Contd)
- Lecture 39 - Shared Memory Architecture, Cache Coherence
- Lecture 40 (Part 1) - Concurrent Programming in Hardware
- Lecture 40 (Part 2) - Concurrent Programming in Hardware
- Lecture 41 - Conclusion :

## Week 12 Assignment

### Assignment Week 12

1) A multi-processor system which at any point of time doesn't need to have multiple processors **1 point** accessing the same memory location is called

- Exclusive Read Exclusive Write PRAM model
- Concurrent Read Inclusive Write PRAM model
- Concurrent Read Concurrent Write PRAM model
- None of the above

#### Accepted Answers:

*Exclusive Read Exclusive Write PRAM model*

2) There is need to ensure synchronization in which of these models

**1 point**

- EREW
- CREW
- CRCW
- All of the above

#### Accepted Answers:

*CRCW*

3) In the case of PRAM, a barrier achieves which of the following

**1 point**

- Processes crosses the barrier as soon as it reaches
- Processes stop execution at the barrier
- Each process waits until another process stops at the barrier
- Each process waits until all the processes complete the execution.

#### Accepted Answers:

*Each process waits until all the processes complete the execution.*

4) Which of these is the characteristic of an optimal algorithm

**1 point**

- No. of processors \* Time < Complexity of best known sequential algorithm
- No. of processors \* Time <= Complexity of best known sequential algorithm
- No. of processors \* Time = Complexity of best known sequential algorithm

Recent Trends  
in Computer  
Organization &  
Architecture

- Quiz : Week 12  
Assignment
- Feedback for  
Week 12
- Week 12  
Solutions

None of the above

**Accepted Answers:**

*No. of processors \* Time = Complexity of best known sequential algorithm*

5) Consider the following scenario. Core P1 holds an address A1 in exclusive state and it is connected to two other processors P2 and P3 through a common bus. There wont be any communication on the bus when

**1 point**

- P1 writes to A1 in P2
- P3 writes to A1 in P3
- P3 writes to A1 in P1
- P1 writes to A1 in P1

**Accepted Answers:**

*P1 writes to A1 in P1*

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