Unit 12 - Week 11

Weekly Assignment

1) In a SMA, if a core A makes a change to a variable b, the state of A is now

- Shared
- Invalid
- Valid
- Exclusive

Accepted Answers:

Exclusive

2) If the value of a variable a in core A and core B is changed in core B, but not reflected in core A, the state of core A is

- Shared
- Invalid
- Valid
- Exclusive

Accepted Answers:

Invalid

3) Multi-programming is achieved efficiently in today's processors using

- DMA
- Caches
- H/W Interrupt
- All of the above

Accepted Answers:

DMA

4) Using time spent on DMA for CPU computation is termed as cycle stealing

- True
- False

Points: 1 point
5) Consider the following scenario. Core P1 holds an address A1 in exclusive state and it is connected to two other processors P2 and P3 through a common bus. There won't be any communication on the bus when

- P1 writes to A1 in P2
- P3 writes to A1 in P3
- P3 writes to A1 in P1
- P1 writes to A1 in P1

Accepted Answers:
P1 writes to A1 in P1

6) In a VIVT (Virtually Indexed Virtually Tagged) Cache, the cache is addressed using

- Physical Address
- Virtual Address
- Cache addressing
- Any of the above

Accepted Answers:
Virtual Address