Thread Level Parallelism - Part 2 (21 AUG 2015 - 28 AUG 2015)

Week8 Quiz 1

The due date for submitting this assignment has passed. Due on 2015-08-28, 23:55 IST.

Submitted assignment

Week8 Quiz

1) lock:  
   ld register,location
   cmp register,#0
   bnz lock
   st location,#1
   ret

unlock:  
   st location,#0
   ret

Considering a multiprocessor environment and each process executing the above code snippet. Choose the option regarding the code snippet

- It is a correct implementation of Mutual Exclusion using “lock” and “unlock” routine.
- It is an implementation of Mutual exclusion but fails to do so as multiple process can enter into critical section due to incorrect check of register value.
- It implements mutual exclusion correctly, but not Barriers.
- It is an implementation of Barriers.

No, the answer is incorrect.

Score: 0

Accepted Answers:

It is an implementation of Mutual exclusion but fails to do so as multiple process can enter into critical section due to incorrect check of register value.

2) Which of the following statements is/are true, while achieving Sequential Consistency through MSI protocol?

I. Read Exclusive bus transaction detects write completion.
II. A read either triggers a bus transaction for obtaining the updated value or it reads the value from the same processor in program order.

- I only
- I and II
- II only
- None

https://onlinecourses.nptel.ac.in/noc15_cs09/unit?unit=18&assessment=74
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3) Which of the following is/are used to achieve synchronization, in a shared memory environment?

I. Locks
II. Barriers
III. Hardware instruction like Load-link/Store-conditional (LL/SC)

No, the answer is incorrect.
Score: 0
Accepted Answers:
I and II

4) If several processes update the same datum concurrently and the outcome of the execution depends on the particular order in which the updation takes place is called

- dynamic condition
- race condition
- essential condition
- critical condition

No, the answer is incorrect.
Score: 0
Accepted Answers:
race condition

5) Which of the following is an important distinction between coherence and consistency?

- Coherence is specified on a per-memory location basis, Consistency is specified with respect to all memory locations.
- Coherence is specified with respect to all memory locations, Consistency is specified on a per-memory location basis.
- Coherence and Consistency are specified on per-memory location basis.
- Coherence and Consistency are specified with respect to all memory locations.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Coherence is specified on a per-memory location basis, Consistency is specified with respect to all memory locations.

6) In a shared memory environment, which of the following statements is/are TRUE.

I. Coherence makes caches invisible
II. Consistency can make a shared memory look like a single memory module
III. Memory consistency models provide rules about loads and stores.
IV. Coherence problem can arise if multiple cores have access to multiple copies of a datum (e.g., in multiple caches) and at least one access is a write.

I, II, III, and IV
7) Which of the following program orders of loads and stores are omitted by a core in TSO (Total Store Order) consistency memory model?

- Load → Load
- Load → Store
- Store → Store
- Store → Load

No, the answer is incorrect.
Score: 0
Accepted Answers: Store → Load

8) Which of the following statements is/are true?
I. FENCE specifies that all instructions before the FENCE in program order must be ordered before any instructions after the FENCE in program order
II. To achieve Sequential Consistency in TSO memory model, FENCE is required between every Store and subsequent Load.

- I only
- II only
- I and II
- None

No, the answer is incorrect.
Score: 0
Accepted Answers: I and II

9) Which of the following statements is correct about SC (sequential Consistency), TSO (Total Store Order), XC (Relaxed Consistency). Here ‘⊂’ represents subset notation.

- SC executions ⊂ TSO executions ⊂ XC executions
- XC executions ⊂ TSO executions ⊂ SC executions
- TSO executions ⊂ SC executions ⊂ XC executions
- SC executions ⊂ XC executions ⊂ TSO executions

No, the answer is incorrect.
Score: 0
Accepted Answers: SC executions ⊂ TSO executions ⊂ XC executions

10) If a program is 100% parallelizable, and all loads and stores in that program are from/to different memory locations. Also, each load and store is accessed only once. If we execute the program on a multi-core system then which memory model is suggestible to get better throughput?

- XC (Relaxed Consistency)
- SC (Sequential Consistency)
- TSO (Total Store Order)
- None
No, the answer is incorrect.
Score: 0
Accepted Answers:
XC (Relaxed Consistency)