Thread Level Parallelism - Multi-Core Processors (12 AUG 2015 - 18 AUG 2015)

Week 7 Quiz 1

The due date for submitting this assignment has passed. Due on 2015-08-18, 23:55 IST.

Submitted assignment

1) Assume that you have a set of programs and each program is 100% parallelizable. Your objective is to run the programs in less amount of time. Which one of the following computer systems gives better throughput?

- One uniprocessor that executes ten billion instructions per second.
- Eight-processor multiprocessor where each processor executes one billion instructions per second.
- Four-processor multiprocessor where each processor executes two billion instructions per second.
- Thousand-processor multiprocessor where each processor executes ten million instructions per second.

No, the answer is incorrect.
Score: 0
Accepted Answers:
One uniprocessor that executes ten billion instructions per second.

2) Suppose a computer program has a method M that cannot be parallelizable, and remaining parts of the program can be parallelized. The method M accounts for 40% of the program's execution time. How much maximum speedup that can be achieved by running the program on a 6-core processor.

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 2

3) In a simultaneous multi-threaded environment, which of the following is/are not shared by threads?

- Program Counter
- Stack
4) Suppose a program creates a binary search tree (BST) with 1000 nodes. We are performing some basic operations (insert, remove, search) on a BST infinitely often by using the program. The probability to perform each operation is the same. If we use the following multi threading technique(s) while performing operations on BST.

I. Coarse-Grain Multi threading
II. Fine-Grain Multi threading

Which multi threading technique(s) give better throughput? (Assume that program is running on a 8-core multiprocessor)

- I only
- II only
- I and II give same throughput
- None

No, the answer is incorrect.
Score: 0
Accepted Answers:
II only

5) What does the term “Non-Uniform” signify in Non Uniform Memory Access (NUMA) architecture.

- Varying memory access latency based on it's location.
- Varying processing elements.
- Varying communication latency.
- None of the above.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Varying memory access latency based on it's location.

6) Consider a multi-core processor using 3-state MSI protocol. If one of the cache block is in S state, what will be the state(s) of the same cache block in other core(s)? (Chosen for Q7)

I. M
II. S
III. I

- I or II or III
- II or III
- II
- III

No, the answer is incorrect.
Score: 0
Accepted Answers:
II or III
7) Suppose an application is running on a 64-processor multiprocessor, which takes 300 cycles to handle reference to a remote memory. If the base CPI is 0.5, how much faster is the multiprocessor if there is no communication versus if 0.3% of the instructions involve a remote communication reference?

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 2.8

8) Consider a multi-core processor using 3-state MSI protocol. Assume that a cache block is shared across all cores. After some time, one of the cores changes the state of the cache block from ‘S’ to ‘M’, what will be the state(s) of the cache block in other cores?

- Modified state.
- Shared state.
- Invalid state.
- Any state.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Invalid state.

9) Necessary conditions for cache coherency to satisfy is/are

- Write propagation.
- Write serialization.
- Program order for memory operations.
- Read serialization.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Write propagation.
Write serialization.
Program order for memory operations.

10) Consider a multicore processor using directory based MSI protocol. One of the cache block is in ‘M’ state. Due to cache replacement, this block is chosen as a victim. What is the next course of action?

- No state transition. Sharers list in home node is unmodified.
- Sharers list in home node is modified to null. State transition to I state.
- The current processor id is removed from sharers list in home node. No state transition.
- State transition to I. Sharers list in home node is unmodified.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Sharers list in home node is modified to null. State transition to I state.