Out-of-order Execution (5 AUG 2015 - 11 AUG 2015)

Week6 Quiz1

The due date for submitting this assignment has passed. Due on 2015-08-11, 23:55 IST.

Submitted assignment

1) Register renaming is done in which of the following stages?  

- Decode stage  
- Dispatch stage  
- Execution stage  
- Write back stage

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
Dispatch stage

2) Consider a superscalar processor with Integer unit (IU), floating-point unit (FU), load-store unit (LU) and branch unit (BU) as functional units. Assume IU is a 3-stage pipeline, FU is a 4-stage pipeline, LU and BU are 3-stage pipelines. Number of slots in reservation station for each functional unit is 5 and number of instructions waiting to complete are 20. What is the maximum number of slots in ROB?

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
(Type: Numeric) 53

3) If a page fault occurs in address translation stage of Load-store unit in a superscalar processor, then

- Process is suspended in the clock cycle itself.  
- Process continues without serving page-fault.  
- Process is suspended after address translation stage.  
- Process is suspended when the instruction that causes the page fault comes to the head of ROB.

No, the answer is incorrect.  
Score: 0  
Accepted Answers:
Process is suspended when the instruction that causes the page fault comes to the head of ROB.

4) Load R0, X
Load R1, Y
Load R3, Z
Add R2, R0, R1
Mul R2, R2, R1
Add R3, R2, R0
Sub R1, R3, R2

Consider a superscalar processor having an integer and load-store unit. Integer unit is a 3-stage pipeline with 1 clock cycle each. Instruction fetch(IF), Instruction decode(ID) and Operand fetch(OF) stages take 1 clock cycle each. Add operation takes 1 clock cycle whereas Mul operation takes 3 clock cycles. Address generation, address translation and memory access stages takes 1 clock cycle each. What is the minimum number of rename registers required for register renaming using RRF?

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 3

5) Spill code is implemented using

- Load instructions.
- Arithmetic instructions.
- Store instructions.
- Branch instructions.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Load instructions.
Store instructions.

6) Preference for load instructions over store instructions in memory access stage is implemented using

- Finished Load Buffer(FLB)
- Finished Store Buffer(FSB)
- Completed Store Buffer(CSB)
- Reordering Buffer(ROB)

No, the answer is incorrect.
Score: 0
Accepted Answers:
Completed Store Buffer(CSB)

7) Operand forwarding is done from

- Execution unit.
- Reordering buffer.
- Write back unit.
- Address register file(ARF).

No, the answer is incorrect.
Score: 0
Accepted Answers:
Execution unit.

8) I1: Load R0, X
I2: Load R1, Y
I3: Mul R2, R0, R1
I4: Store Z, R2
I5: Add R2, R0, R1
I6: Store Z, R2

The above program is executed on a superscalar processor having two Integer units (IU1, IU2) and load-store unit (LSU) as functional units. The memory locations X and Y contains 10 and 7 respectively. What will be the value stored in the register R2 after the writeback of I4?

- 17
- 70
- 87
- Invalid

No, the answer is incorrect.
Score: 0
Accepted Answers: Invalid

9) Alias bit is set to 1 if there is _________ dependency between store and load instructions. 1 point

- RAW due to memory locations.
- RAW due to registers.
- Both A & B.

No, the answer is incorrect.
Score: 0
Accepted Answers: RAW due to memory locations.

10) If an interrupt occurs, 1 point

- Process is suspended.
- All stores in CSB are saved to memory.
- All architectural registers are saved.
- Entire pipeline is flushed.

No, the answer is incorrect.
Score: 0
Accepted Answers: Process is suspended.
All stores in CSB are saved to memory.
All architectural registers are saved.

11) Load forwarding refers to 1 point

- Bypassing earlier stores.
- Preference to store over the load.
- Store can forward data to a later load.
- Preference to load over the store.

No, the answer is incorrect.
Score: 0
Accepted Answers: Store can forward data to a later load.

12) Once a reservation station entry is made for an instruction, can the entry be deallocated? [Yes/No] 1 point

- Yes
- No

No, the answer is incorrect.
Score: 0
13) In a superscalar processor load instructions executed speculatively i.e, irrespective of dependencies with store instructions. [True/False]

- True
- False

No, the answer is incorrect.
Score: 0

Accepted Answers:
True

14) Which of the following phases occur in the dispatch stage?

- Renaming of registers.
- Allocating of entry in Reservation station and ROB.
- Advancing instruction buffer from ROB to RS.
- None of the above.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Renaming of registers.
Allocating of entry in Reservation station and ROB.