Instruction Level Parallelism (29 JUL 2015 - 04 AUG 2015)

Week5 Quiz 1

The due date for submitting this assignment has passed. Due on 2015-08-04, 23:55 IST.

Submitted assignment

1) Which of the following dependency causes a stall, in scalar processor execution? 1 point

- WAW dependence
- WAR dependence
- RAW dependence
- None of the above

No, the answer is incorrect.

Score: 0

Accepted Answers:
- RAW dependence

2) Which of the following are TRUE in the context of compiler optimizations for exposing Instruction Level Parallelism (ILP)? 1 point

- Separate the execution of a dependent instruction from the source instruction by the pipeline depth.
- Replicate the loop body multiple times and adjust the loop terminating condition.
- Identify independent instructions and schedule them appropriately.
- Identify dependent instructions and schedule them appropriately.

No, the answer is incorrect.

Score: 0

Accepted Answers:
- Separate the execution of a dependent instruction from the source instruction by the pipeline depth.
- Replicate the loop body multiple times and adjust the loop terminating condition.
- Identify independent instructions and schedule them appropriately.
- Identify dependent instructions and schedule them appropriately.

3) Which of the following options give correct branch prediction outcome? 1 point

T: stands for branch taken
N: stands for branch not-taken

a=0;


```c
while(a<10)
{
B1: if(a%2==0)
    a=a+3;
B2: if(a%2==1)
    a=a+2;
}
```

- B1: TTN  B2:TNT
- B1: TNN  B2:TTT
- B1: TNT  B2:NTN
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
B1: TNN  B2:TTT

4) Consider the below code:
```c
int k=0;
for(i=0;i<M;i++){
    for(j=0;j<N;j++)
    {
        k+=2;
        cout<<k;
    }
}
```

Using 2-bit branch predictor what is the misprediction rate for the inner for loop? Assume that the counters are initialized to 00 state (Prediction not taken).

- 1/M(N+1)
- 1/MN
- 1/N
- 1/(N+1)

No, the answer is incorrect.
Score: 0

Accepted Answers:
1/(N+1)

5) 
```
ADD R0,R1,R2
MUL R3,R0,R4
SUB R1,R5,R3
```

Identify type of data hazards in above 3-address code where 1st register is the destination operand register and remaining two are source operand registers.

- RAW, WAR, RAR
- RAW, WAW
- RAW, WAR
- WAR, RAW, WAW

No, the answer is incorrect.
Score: 0

Accepted Answers:
RAW, WAR

6) Assertion : Loop unrolling fails in exposing ILP if data dependencies are present in the loop.
Reason: If data dependencies are present in the instruction, then the instruction cannot be pipelined and executed in parallel.

- Assertion is true but reason is false.
- Assertion is false but reason is true.
- Assertion and reason are true and reason explains it.
- Assertion and reason true but reason doesn't explain it.
- Both are false.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Assertion and reason are true and reason explains it.

7) Which prediction technique gives best performance for the above mentioned for loop?

- Static prediction - Always Taken
- Static prediction - Always Not taken
- Dynamic 1-bit prediction with initial prediction as branch taken
- All are same

No, the answer is incorrect.
Score: 0

Accepted Answers:
Static prediction - Always Not taken

8) Load R0, M
   Load R1, N
   stall
   ADD R2, R0, R1
   SUB R3, R0, R2
   Load R4, 16(R3)
   stall
   MUL R5, R2, R4

In the above code the stall cycles can be removed by pipeline scheduling. State whether the statement is true/false.

- True
- False

No, the answer is incorrect.
Score: 0

Accepted Answers:
False

9) Statement 1: In static branch prediction if the prediction is branch taken, in the ID stage flush the pipeline and load the program counter with predicted branch target address.

Statement 2: In static branch prediction if the prediction is branch not taken but if branch is taken in EX stage, then flush the pipeline in EX stage and load the program counter with predicted branch target address.

- Statement 1 is true but Statement 2 is false
- Statement 1 is false but Statement 2 is true
- Both statements are true
- Both statements are false

No, the answer is incorrect.
Score: 0

Accepted Answers:
Both statements are true

10) Consider the following code:
    Load R1,M
    Load R2,N
    CMP R1,R2
    JGE END
    Store [300], R2
    END: Store [300], R1

    Assume that M=30 and N=25. The above sequence of instructions is to be executed on a pipelined processor with IF, ID, OF, EX and WB stages. OF refers to operand fetch i.e., register read of operand. Operand forwarding and static branch prediction with prediction not taken are considered. The IF, ID, OF and WB stages take 1 clock cycle each for all instructions. The EX stage takes 2 clock cycles for CMP instruction, and 1 clock cycle for all other instructions. The branch outcome is known after EX stage. Determine the number of clock cycles required for completion of execution of all instructions.

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 13