Fundamentals of Pipelining (22 JUL 2015 - 28 JUL 2015)

Week4 Quiz1

The due date for submitting this assignment has passed. Due on 2015-08-04, 23:55 IST.

Submitted assignment

1) What will be the optimal pipeline depth if A and B are the cost and latency of a non-pipelined design, and C and D are the cost and delay of a latch?

- SQRT(AC/BD)
- SQRT(CD/AB)
- SQRT(AB/CD)
- SQRT(BD/AC)

No, the answer is incorrect.
Score: 0
Accepted Answers:
SQRT(AB/CD)

2) T1 is the time taken by first instruction to complete in a non-pipeline system, and T2 is the time taken by first instruction to complete in a pipeline system with inter-stage buffer registers. What is the relationship between T1 and T2?

- T1<T2
- T1>=T2
- T1=T2
- T1>T2

No, the answer is incorrect.
Score: 0
Accepted Answers:
T1<T2

3) An instruction pipeline has a single functional unit to perform arithmetic operations. It consists of 4 stages to implement three instructions (ADD, MUL, SUB). All stages, except the execution stage, take 1 clock, while the execution stage for ADD and SUB takes 2 clocks each and for MUL it takes 3 clocks. If all the instructions are executed in the above order, how many clocks are required to complete these 3 instructions?

- 7
- 8
- 9
4) Given a non-pipelined architecture running at 1GHz, that takes 5 cycles to finish an instruction. You want to make it pipelined with 5 stages. The increase in hardware forces you to run the machine at 800MHz. The only stalls are caused by memory and branch instructions. 25% of the total instructions are memory instructions and a stall of 70 cycles happens in 2% of the memory instructions. 20% of the total instructions are branch instructions and a stall of 2 cycles happens in 10% of the branch instructions. What is the speedup that can be achieved with pipelining as compared to non-pipelined design?

No, the answer is incorrect.
Score: 0
Accepted Answers: 2.87

5) In a 5-stage instruction pipeline (IF, ID, OF, EX, WB), a single functional unit performs all arithmetic operations. Here, OF indicates the Operand Fetch stage. All the pipeline stages other than execute stage will take 1 clock cycle per stage, while the execute stage will take 1 clock cycle for ADD and SUB, 3 clock cycles for MUL and 6 clocks for DIV. If operand forwarding is allowed, what will be the minimum number of clocks required to complete the following four instructions?

I1: MUL R2, R0, R1
I2: DIV R5, R3, R4
I3: ADD R2, R5, R2
I4: SUB R5, R2, R6

No, the answer is incorrect.
Score: 0
Accepted Answers: 15

6) Consider two pipelines having the same number of stages and support overlapping of all instructions except memory instructions. In case, if two memory operations cannot be done simultaneously, there will be a 1-cycle penalty. 35% instructions are memory instructions. Single port memory is considered for pipeline1 while dual-port memory is considered for pipeline2. What is the speedup achieved with pipeline2 with respect to pipeline1?

No, the answer is incorrect.
Score: 0
Accepted Answers: 1.35
7) In a 5-stage instruction pipeline, all instructions can be overlapped except the branch instructions. In case of a branch instruction, the target instruction will not be fetched until the branch instruction is completed. If there are 30% branch instructions, what is the effective speedup factor of the pipeline with 1GHz clock?

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: String) 2.27

8) A CPU has 5 pipeline stages. A branch target is known at the end of the third stage. There are 20% branch instructions. The program has $10^9$ instructions, where each non-branch instruction on an average takes 1 clock. What will be the average CPI (clocks per instruction)?

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 1.4

9) In an instruction pipeline of 5-stages, it is found that the branch instructions incur 3 stalls, data dependences incur 2 stalls, and the memory operations incur 1 stall. In a given program, we have 12% of the instructions as branches, 12% of the instructions as memory operations, 36% of the instructions as ALU instructions with data dependence, and the remaining 40% of the instructions as ALU instructions with no dependency. How many clock cycles are required to complete this program?

- 220
- 240
- 340
- 216

No, the answer is incorrect.
Score: 0
Accepted Answers:
220

10) Source(s) of stall in a pipelined processor is/are

- Structural dependency
- Control dependency
- Data dependency
- All of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
All of the above

11) If the time taken to complete a stage in a pipeline is less than the clock period, it leads to

- External fragmentation
- Internal fragmentation
- Stall
- None of the above
Control dependency can be handled using below technique(s):

- Multiple pipelines.
- Delayed load.
- Branch prediction.
- Operand forwarding.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Multiple pipelines.
Delayed load.
Branch prediction.

A. Internal fragmentation
B. External fragmentation
C. Pipeline stalls

A. Reduce the complexity of different instructions
B. Dependent computations
C. Minimizing addressing modes

No, the answer is incorrect.
Score: 0
Accepted Answers:
A-c,B-a,C-b