Week2 Quiz

The due date for submitting this assignment has passed. Due on 2015-07-28, 23:55 IST.

Submitted assignment

1) Consider a memory system with a single L1 cache that has an average access time of 100ns without L1, and 30ns with L1. L1 has an access time of 10ns. What is the hit ratio of L1 required to have an average access time of 30ns.

- 90%
- 70%
- 80%
- 81.8%

No, the answer is incorrect.
Score: 0
Accepted Answers:
80%

2) Consider a memory system with I-cache, D-cache, L2 cache and main memory access time of 5ns, 5ns, 10ns and 100ns respectively, and their respective hit ratios are 0.85, 0.80, 0.9 and 1. On executing a program, 40% of instructions access I-cache and 60% of instructions access D-cache. What is the average memory access time?

- 6.6ns
- 14.7ns
- 8.6ns
- 12.2ns

No, the answer is incorrect.
Score: 0
Accepted Answers:
8.6ns

3) For the above question, What is the throughput (i.e., the number of instructions executed per second)

MIPS - Millions of Instructions per Second

- 166 MIPS
4) Which of the following statement/s is/are FALSE?
I: In set associative mapping, if set size is reduced to 1; it reduces to fully associative mapping.
II: In set associative mapping if only one set is present, it reduces to direct mapping.

- I Only
- II Only
- Both I and II
- None

No, the answer is incorrect.
Score: 0
Accepted Answers:
Both I and II

5) Which of the following is true?
I: Write back updation of cache leads to raw hazards
II: Write through mechanism reduces the average memory access time
III: Write back and write through mechanisms reduce conflict misses
IV: Write back and write through mechanisms maintain cache coherence

- I, II, and IV
- I, and IV
- I, II, and III
- Only IV is True

No, the answer is incorrect.
Score: 0
Accepted Answers:
I, and IV

6) Consider a system with following sequence of memory block accesses: 16, 0, 16, 0, 4, 0, 4. Cache memory has 16 blocks and main memory has 64 blocks. In this case which of the below mapping techniques result in least number of misses and less hardware complexity (i.e., least number of tag comparators)?

- Direct mapping
- 2-way set associative
- 4-way set associative
- Fully associative

No, the answer is incorrect.
Score: 0
Accepted Answers:
2-way set associative

7) Consider a system with a block size of p words. What is the range of words present in the kth block of main memory?

- \( k \cdot p \) to \((k+1) \cdot p - 1\)
- \( k \cdot p^2 \) to \((k+1) \cdot p^2 \)

No, the answer is incorrect.
8) A computer has a 512KB, 8-way set associative data cache with block size of 32B. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition to the address tag, 2 valid bits, 1 modified bit and 1 replacement bit.
A. what will be the number of tag bits?

- 11
- 16
- 21
- 12

No, the answer is incorrect.
Score: 0
Accepted Answers:
k*p to (k+1)*p - 1

9) B. What will be the cache controller size?

- 40KB
- 320KB
- 192KB
- 32KB

No, the answer is incorrect.
Score: 0
Accepted Answers:
40KB

10) The following program fragment is executing on a single core machine
    for(int i=0; i<n; i++)
    sum = sum + A[i]

Which of the following updation techniques of the cache will result in less access time of the variables 'i' and 'sum' respectively?

- write back to i and write through
- write through for i and write back for sum
- write through for both i and sum
- write back for both i and sum

No, the answer is incorrect.
Score: 0
Accepted Answers:
write back for both i and sum

11) Consider n unique memory block accesses on a fully associative cache with k blocks.
What is the necessary relation required to ensure maximum number of misses using FIFO replacement policy?

- n=k+1
- n<k
- n=k
- n<=k

No, the answer is incorrect.
Score: 0
12. Which of the following statement(s) is/are TRUE for non-blocking cache?

- Increases complexity of cache controller
- May require pipelined or bank system
- Results in multiple outstanding memory accesses
- Allows cache access during miss handling.
- Increases effective miss penalty

No, the answer is incorrect.
Score: 0

Accepted Answers:
Increases complexity of cache controller
May require pipelined or bank system
Results in multiple outstanding memory accesses
Allows cache access during miss handling.

13. A cache with tag array access time of 12ns and data array access time of 10ns. If the tag comparator delay is 5ns, write buffer access time is 3ns and parallel cache access mode i.e., tag and data array are accessed in parallel is used then the cache access time is ________ microseconds. (Neglect set decoding and data input time.)

- 20
- 0.02
- 18
- 0.18

No, the answer is incorrect.
Score: 0

Accepted Answers:
0.02

14. Match the following

A. Capacity Misses  I. Fully Associative cache
B. Compulsory Misses II. Set Associative cache
C. Conflict Misses   III. Direct Mapped cache
IV. Cold Start cache

- A. III, B. IV, C. II
- A. I, B. I, C. II and III
- A. I, B. IV, C. II and III
- A. I, B. II, C. III

No, the answer is incorrect.
Score: 0

Accepted Answers:
A. I, B. IV, C. II and III