Instruction Set Architecture (JUL 1 2015 - JUL 7 2015)

Course outline

Introduction to Computer Architecture

Instruction Set Architecture (JUL 1 2015 - JUL 7 2015)

- Quantitative Principles of Computer Design
- Instruction Set Principles-Part 1
- Instruction Set Principles-Part 2
- Instruction Set Principles-Part 3

Memory Hierarchy Design - Cache Memory Hierarchy (8 JUL 2015 - 14 JUL 2015)

Memory Hierarchy Design - Main Memory Design (15 JUL 2015 - 21 JUL 2015)

Fundamentals of Pipelining (22)

Week1 Quiz 1

The due date for submitting this assignment has passed. Due on 2015-07-28, 23:55 IST.

Submitted assignment

1) I. In Load-store architecture, any instruction can use immediate addressing mode.
II. In Load-store architecture, any instruction can use direct addressing mode.
III. In Load-store architecture, memory elements can be accessed only through load and store instruction.

- I is true since III is true
- I is true since III is false
- II is false since III is true
- II is true since III is false

No, the answer is incorrect.
Score: 0

Accepted Answers:
II is false since III is true

2) Assume that an ISA supports 32-bit instructions and uses word addressable memory. Each word takes 8 bytes of space. If the ISA supports 32-bit registers and 8-bit operands, what will be the maximum value that an instruction can access by using operand reference, with immediate, register, and direct addressing modes, respectively?

- 2^32-1, 2^32-1, 2^64-1
- 2^8-1, 2^8-1, 2^32-1
- 2^8-1, 2^32-1, 2^64-1
- 2^32-1, 2^32-1, 2^32-1

No, the answer is incorrect.
Score: 0

Accepted Answers:
2^8-1, 2^32-1, 2^64-1

3) Select the statement(s) below that is/are TRUE.

- We can achieve position independence (Relocatable code) by using indexed addressing mode.
- Indirect addressing mode is useful to swap to contents in memory.
- Relative Addressing mode is used for position independence.
- Indexed, relative addressing modes are used to access array elements.

Score: 0

Accepted Answers:
4) An instruction should have at least

- One Operand
- Two Operands
- Three Operands
- None

No, the answer is incorrect.  
Score: 0

Accepted Answers:
None

5) The number of instructions needed to add 9 numbers in 1-operand addressing mode (including load and store instructions)

No, the answer is incorrect.  
Score: 0

Accepted Answers:
(Type: Numeric) 10

6) Assume indirect addressing mode is used with n levels of indirection. How many memory accesses are required to obtain the target value?

- n
- n-1
- n+1
- 1
- none

No, the answer is incorrect.  
Score: 0

Accepted Answers:
n+1

7) In a system the contents of PC, Base register, Register R0, and Register R1 has contents 60, 100, 10, and 20, respectively. Content of R1 is used as the displacement value. What is the effective address computed using the Base addressing and the Relative-Base addressing modes, respectively?

- 120, 80
- 110, 120
- 120, 160
- 120, 180

No, the answer is incorrect.  
Score: 0

Accepted Answers:
120, 180

8) Which of the following addressing modes are suitable for data encapsulation?

- Immediate
- Index
- Indirect

No, the answer is incorrect.  
Score: 0

Accepted Answers:
1 point
9) Compiler and ISA jointly affects the following

- Instruction count and CPI
- CPI and clock cycle time
- Instruction count and clock cycle time
- CPI

No, the answer is incorrect.
Score: 0
Accepted Answers:
Instruction count and CPI

10) A basic computer system with a single core processor where memory operations take 40% of execution time. An enhancement called L1 cache speeds up 60% of memory operations by a factor of 4. Another enhancement called L2 cache speeds up half of remaining 40% of memory operations by a factor of 2. What is overall speedup of system? (Round off to 3 decimal digits)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 1.282

11) CISC architecture
   a. Symmetric registers
   b. Multiple memory references
   c. Condition code register
   d. Single memory reference

No, the answer is incorrect.
Score: 0
Accepted Answers:
i-a,ii-c,iii-b,iv-d
i-c,ii-a,iii-b,iv-d
i-c,ii-a,iii-b,iv-b
i-c,ii-a,iii-d,iv-b

12) I : Data transfer between two machines which both supports only 8 byte words doesn’t require alignment.
II : Data transfer between two machines in which one of the system supports only 8 byte words and the other supports only 1 byte words requires alignment.
III : Data transfer between two machines in which one of the system supports only 8 byte words and the other machine supports only 4 byte words requires alignment.

Which of the following options is true according to the memory access time?
None of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
I<II<III