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Unit 4 - Week 2

Assignment 2

The due date for submitting this assignment has passed. Due on 2020-02-12, 23:59 IST.
As per our records you have not submitted this assignment.

1) Write the Vector Code(VMIPS) for the given C code- ***15 points***

```
X = X + a * Y
```

Options:

A)

```
L.D F0,a
LV V1,Ry
MULVS.D V2,V1,F0
LV V3,Rx
ADDVV.D V4,V2,V3
SV V4,Rx
```

B)

```
L.D F0,a
LV V1,Rx
MULVS.D V2,V1,F0
LV V3,Ry
ADDVV.D V4,V2,V3
SV V4,Ry
```

C)

```
LI VLR, a
LV V1, R1
LV V2, R2
MULVS.D V2,V1,F0
ADDV.D V3, V1, V2
SV V3, R3
```

D)

```
LI VLR, a
LV V1, R1
LV V2, R2
ADDV.D V3, V1, V2
SV V3, R3
```

- A.
- B.
- C.
- D.

No, the answer is incorrect.
Score: 0

Accepted Answers:
A.

2)

For the following code, which multiplies two vectors of length 300 that contain single-precision complex values, what is the arithmetic intensity of this kernel (i.e., the ratio of floating-point operations per byte of memory accessed)?

```
for (i=0; i<300; i++)
{
      c_re[i] = a_re[i] * b_re[i]  – a_im[i] * b_im[i];
      c_im[i] = a_re[i] * b_im[i] + a_im[i] * b_re[i];
}
```

No, the answer is incorrect.
Score: 0

Accepted Answers:
(Type: Numeric) 1

15 points

3)

Assume a hypothetical GPU with the following characteristics:

- **Clock rate 1.5 GHz**
- **Contains 16 SIMD processors, each containing 32 single-precision floating point units**

What is the peak single-precision floating-point throughput for this GPU in GLFOPs/sec, assuming that all memory latencies can be hidden?

No, the answer is incorrect.
Score: 0

Accepted Answers:
(Type: Numeric) 768

15 points

4) ***5 points***

Which of the following architecture is not suitable for realizing SIMD ?

A. Vector Processing Architecture
B. GPGPU Architecture
C. Von Neumann Architecture
D. All of the above

- A.
- B.
- C.
- D.

No, the answer is incorrect.
Score: 0

Accepted Answers:
C.

5) _____ handles Data Level Parallelism. ***5 points***

a) Register
b) Cache
c) Data BUS
d) Vector Processor

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

6) Vector Processors contain both scalar and vector registers. ***5 points***

A. True
B. False

- A.
- B.

No, the answer is incorrect.
Score: 0

Accepted Answers:
A.

7) State which statement is true. ***5 points***

a) Tesla GeForce 8800 has total 128 SP organized in 8 SM
b) Tesla GeForce 8800 has total 8 SP organized in 128 SM
c) Tesla GeForce 8800 has total 128 SP organized in 16 SM
d) Tesla GeForce 8800 has total 16 SP organized in 128 SM

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.

8) ***5 points***

Match the functionalities of different shader programs with appropriate shader-

a) Vertex Shader
b) Pixel Shader
c) Geometry Shader

i) Map the position of vertices onto the screen, altering their position, color, or orientation
ii) Operate on lines and triangles defined by multiple vertices, changing or generating additional primitives
iii) Fills the interior of primitives, including interpolating per-fragment parameters, texturing, and coloring
iv) Depth testing and stencil testing, color blending operation etc

Select the correct option.

A. a -> i,b->iii,c->ii
B. a -> ii,b->i,c->iii
C. a -> i,b->ii,c->iii
D. a -> ii,b->iii,c->i

- A.
- B.
- C.
- D.

No, the answer is incorrect.
Score: 0
Accepted Answers:
A.

9) GPUs are _____-oriented Processors. ***5 points***

a) Latency
b) Throughput
c) Processor Utilisation
d) None of the above

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

10) ***5 points***

The world's first GPU is _____ introduced in _____.

a) GeForce 256, 1999
b) GeForce 8800, 2000
c) GeForce 100, 1990
d) GeForce 80 , 1980

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.

11) ***5 points***

Primary design objective for Tesla architecture is _____.

a) Increase latency for high-precision math operations
b) Decrease latency for low-precision texture filtering
c) Depth testing and stencil testing, color blending operation etc
d) Execute vertex and pixel-fragment shader programs on the same unified processor

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

12 PTX instructions have format: opcode.type d, a, b, c; where d is the ***5 points***

A. Destination
B. Domain
C. Data
D. Double

- A.
- B.
- C.
- D.

No, the answer is incorrect.
Score: 0

Accepted Answers:
A.

13 GPGPU programming use _____ execution model. ***5 points***

a) SISD
b) SIMD
c) MISD
d) MIMD

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

14) ***5 points***

Which of the following statements is correct.

A. Compared to CPU, GPUs have larger register file, smaller L1/L2 cache with higher bandwidth
B. Compared to CPU, GPUs have smaller register file, smaller L1/L2 cache with lower bandwidth
C. L1 and L2 cache + Shared memory is private to SMs
D. Cache + Constant memory is unified for all SMs

- A.
- B.
- C.
- D.

No, the answer is incorrect.
Score: 0

Accepted Answers:
A.