Assignment 1

The due date for submitting this assignment has passed. Due on 2020-02-12, 23:59 IST. As per our records you have not submitted this assignment.

1) A non-pipelined processor was redesigned as a 5 stage pipelined processor. The different stages have latencies as shown in the following table.

<table>
<thead>
<tr>
<th></th>
<th>Fetch</th>
<th>Decode</th>
<th>Execute</th>
<th>Memory</th>
<th>Writeback</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300ps</td>
<td>400ps</td>
<td>350ps</td>
<td>500ps</td>
<td>100ps</td>
</tr>
</tbody>
</table>

Further assume that each pipeline stage incurs an extra 20ps (picosecond $10^{-12}$) latency on account of the registers between pipeline stages.

What is the cycle time and the latency of an instruction for the non-pipelined and pipelined processors? Your answer should contain the quantities in the following order: (non-pipelined cycle time, non-pipelined latency, pipelined cycle time, pipelined latency)

Options:
A) 1650ps, 2600ps, 1650ps, 2600ps
B) 1650ps, 1650ps, 520ps, 2600ps
C) 1650ps, 3300ps, 1645ps, 2600ps
D) 1650ps, 2000ps, 310ps, 2600ps

A. 
B.
2) A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

Options:
- Tag, Block, and Word
- A) 5, 6, 5
- B) 6, 4, 5
- C) 5, 5, 6
- D) 6, 5, 4

No, the answer is incorrect.
Score: 0
Accepted Answers:

C.

3) Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

a) A
b) B
c) Both take the same time
d) Insufficient information

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.

4) When performing a looping operation, the instruction gets stored in the ________

a) Registers
b) Cache
c) System Heap
d) System stack

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.
d.
No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

5) **An 24 bit address generates an address space of _____ locations.**
   a) 1024
   b) 4096
   c) 1048576
   d) 16,777,216
   d.
No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

6) **The computer architecture aimed at reducing the time of execution of instructions is _____**
   a) CISC
   b) RISC
   c) ISA
   d) ANNA
   d.
No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

7) **The contention for the usage of a hardware device is called _____ and the situation wherein the data of operands are not available is called _____**
   a) Structural hazard, Data hazard
   b) Data hazard, Structural hazard
   c) Deadlock, Stock
   d) Stock, Deadlock
   a.
No, the answer is incorrect.
Score: 0
Accepted Answers:
a.
8) 10 points
Pipelining increases CPU instruction \underline{\underline{\text{_________}}} and reduces processor's \underline{\underline{\text{_________}}}.

\begin{itemize}
\item a) Size, Efficiency
\item b) Throughput, Cycle time
\item c) Cycle rate, Cycle time
\item d) Latency, Efficiency
\end{itemize}

\begin{itemize}
\item a.
\item b.
\item c.
\item d.
\end{itemize}

No, the answer is incorrect.
Score: 0
Accepted Answers: 
\text{b.}

9) 10 points
One of the possible ways to deal with data hazards is \underline{\underline{\text{_________}}}.

\begin{itemize}
\item a) Reducing CPI
\item b) Using branch prediction
\item c) Increasing number of processors
\item d) Adding forwarding hardware
\end{itemize}

\begin{itemize}
\item a.
\item b.
\item c.
\item d.
\end{itemize}

No, the answer is incorrect.
Score: 0
Accepted Answers: 
\text{d.}

10) 0 points
Branch decision is inferred in \underline{\underline{\text{_________}}} stage.

\begin{itemize}
\item a) Fetch
\item b) Decode
\item c) Mem
\item d) Write back
\end{itemize}

\begin{itemize}
\item a.
\item b.
\item c.
\item d.
\end{itemize}

No, the answer is incorrect.
Score: 0
Accepted Answers: 
\text{c.}