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Unit 3 - Week 1

Assignment 1

The due date for submitting this assignment has passed. Due on 2020-02-12, 23:59 IST.
As per our records you have not submitted this assignment.

1) ***10 points***

A non-pipelined processor was redesigned as a 5 stage pipelined processor. The different stages have latencies as shown in the following table.

Fetch	Decode	Execute	Memory	Writeback
300ps	400ps	350ps	500ps	100ps

Further assume that each pipeline stage incurs an extra 20ps (picosecond 10^{-12}) latency on account of the registers between pipeline stages.

What is the cycle time and the latency of an instruction for the non-pipelined and pipelined processors ? Your answer should contain the quantities in the following order:
(non-pipelined cycle time, non-pipelined latency, pipelined cycle time, pipelined latency)

Options:
A) 1650ps, 2600ps, 1650ps, 2600ps
B) 1650ps, 1650ps, 520ps, 2600ps
C) 1650ps, 3300ps, 1645ps, 2600ps
D) 1650ps, 2000ps, 310ps, 2600ps

- A.
- B.

C.
D.

No, the answer is incorrect.
Score: 0

Accepted Answers:
B.

2) ***10 points***

A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

Options:
Tag, Block, and Word
A) 5, 6, 5
B) 6, 4, 5
C) 5, 5, 6
D) 6, 5, 4

A.
B.
C.
D.

No, the answer is incorrect.
Score: 0

Accepted Answers:
C.

3) ***10 points***

Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?
a) A
b) B
c) Both take the same time
d) Insufficient information

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.

4) ***10 points***

When performing a looping operation, the instruction gets stored in the _____
a) Registers
b) Cache
c) System Heap
d) System stack

a.
b.
c.

d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

5) **An 24 bit address generates an address space of _____ locations.** ***10 points***

a) 1024
b) 4096
c) 1048576
d) 16,777,216

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

6) ***10 points***

The computer architecture aimed at reducing the time of execution of instructions is _____
a) CISC
b) RISC
c) ISA
d) ANNA

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

7) ***10 points***

The contention for the usage of a hardware device is called _____and the situation wherein the data of operands are not available is called _____

a) Structural hazard, Data hazard
b) Data hazard, Structural hazard
c) Deadlock, Stock
d) Stock, Deadlock

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.

8) ***10 points***

Pipelining increases CPU instruction _____ and reduces processor's _____.

a) Size, Efficiency
b) Throughput, Cycle time
c) Cycle rate, Cycle time
d) Latency, Efficiency

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

9) **One of the possible ways to deal with data hazards is _____.** ***10 points***

a) Reducing CPI
b) Using branch prediction
c) Increasing number of processors
d) Adding forwarding hardware

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

10 **Branch decision is inferred in_____ stage.** ***0 points***

a) Fetch
b) Decode
c) Mem
d) Write back

- a.
- b.
- c.
- d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.