Unit 11 - Week 9

Course outline

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Week 9 Assignment 9

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-10-02, 23:59 IST.

1) What is the main application of PISO and SIPO registers? 1 point

a. For data storage
b. For parallel data communication
c. For serial data communication
d. None of these

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

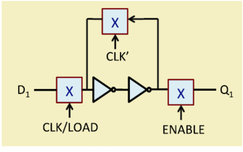
2) What is the function of the LOAD input of a PIPO register? 1 point

a. To store the data in the register in synchronism with a clock.
b. To force the outputs to the high impedance state when required.
c. To enable or disable the shift register functionality.
d. None of these.

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.

3) What are the features of the following CMOS storage cell? 1 point



a. Data is stored as charge on a tiny capacitor.
b. The data gets refreshed in synchronism with the clock.
c. It implements static storage.
d. None of these.

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.
b.

4) The number of additional NAND gates required to construct a 4-bit shift register using J-K flip-flops is ....., assuming that the serial input (SI) is available in both complemented and un-complemented forms. 1 point

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 0

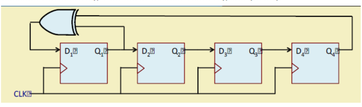
5) A 16-bit ring counter and a 16-bit Johnson counter will respectively count modulo 1 point

a. 16 and 16
b. 16 and 32
c. 32 and 16
d. None of these

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

6) Consider the following 4-bit linear feedback shift register (LFSR): 0 points



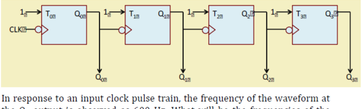
The register is initialized with $D_4 = 1$, $D_3 = D_2 = D_1 = 0$. What will be the state of the register ($Q_4\ Q_3\ Q_2\ Q_1$) after 8 clock pulses are applied?

a. 1001
b. 0110
c. 1100
d. 0100

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.

7) Consider a 4-bit ripple counter as follows: 1 point



In response to an input clock pulse train, the frequency of the waveform at the Q_0 output is observed as 600 Hz. What will be the frequencies of the waveforms at the Q_1 and Q_3 outputs?

a. 1200 Hz and 4800 Hz
b. 300 Hz and 75 Hz
c. 300 Hz and 150 Hz
d. None of these

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

8) In an down-counting ripple counter, 1 point

a. The first flip-flop from the left changes state every clock pulse.
b. The second flip-flop from the left changes state every 2 clock pulses.
c. The third flip-flop from the left changes state every 4 clock pulses.
d. All of these.

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

9) In a 5-bit ripple counter, the number of transient states when moving from the count values 11111 to 00000 will be 1 point

a. 3
b. 4
c. 5
d. None of these

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

10) Three binary ripple counters, modulo-A, modulo-B and modulo-C respectively, are connected in cascade. For counting modulo-500, which of the following are correct solutions? 1 point

a. A = 10, B = 10, C = 5
b. A = 150, B = 200, C = 150
c. A = 25, B = 2, C = 10
d. A = 10, B = 20, C = 25

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.
c.