

# Unit 10 - Week 8

## Course outline

How to access the portal

Week 0 Assignment 0

Week 1

Week 2 : Unit 2

Week 3 : Unit 3

Week 4 : Unit 4

Week 5 : Unit 5

Week 6

Week 7

Week 8

Lecture 36 : Synthesis of Synchronous Sequential Circuits (Part I)

Lecture 37 : Synthesis of Synchronous Sequential Circuits (Part II)

Lecture 38 : Synthesis of Synchronous Sequential Circuits (Part III)

Lecture 39 : Synthesis of Synchronous Sequential Circuits (Part IV)

Lecture 40 : Minimization of Finite State Machines (Part I)

Lecture 41 : Minimization of Finite State Machines (Part II)

Lecture Materials

Feedback for Week 8

Quiz : Week 8 Assignment 8

Week 9

Week 10

Week 11

Week 12

Download Videos

Text Transcripts

Detail Solution

Live Session

## Week 8 Assignment 8

The due date for submitting this assignment has passed.  
As per our records you have not submitted this assignment.

Due on 2019-09-25, 23:59 IST.

- 1) Which of the following statements are true?
- In a synchronous sequential circuit, all state changes occur in synchronism with a clock pulse.
  - In an asynchronous sequential circuit, all state changes occur in synchronism with a clock pulse.
  - In a synchronous sequential circuit, all state changes occur depending on the delays of the circuit elements.
  - In an asynchronous sequential circuit, all state changes occur depending on the delays of the circuit elements.

1 point

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.  
Score: 0

Accepted Answers:  
a.  
d.

- 2) What does the state transition diagram indicate?
- How states change and outputs generated in response to various inputs.
  - The behavior of the different states in terms of their transient behaviors.
  - The input-output behavior of a combinational circuit.
  - None of these.

1 point

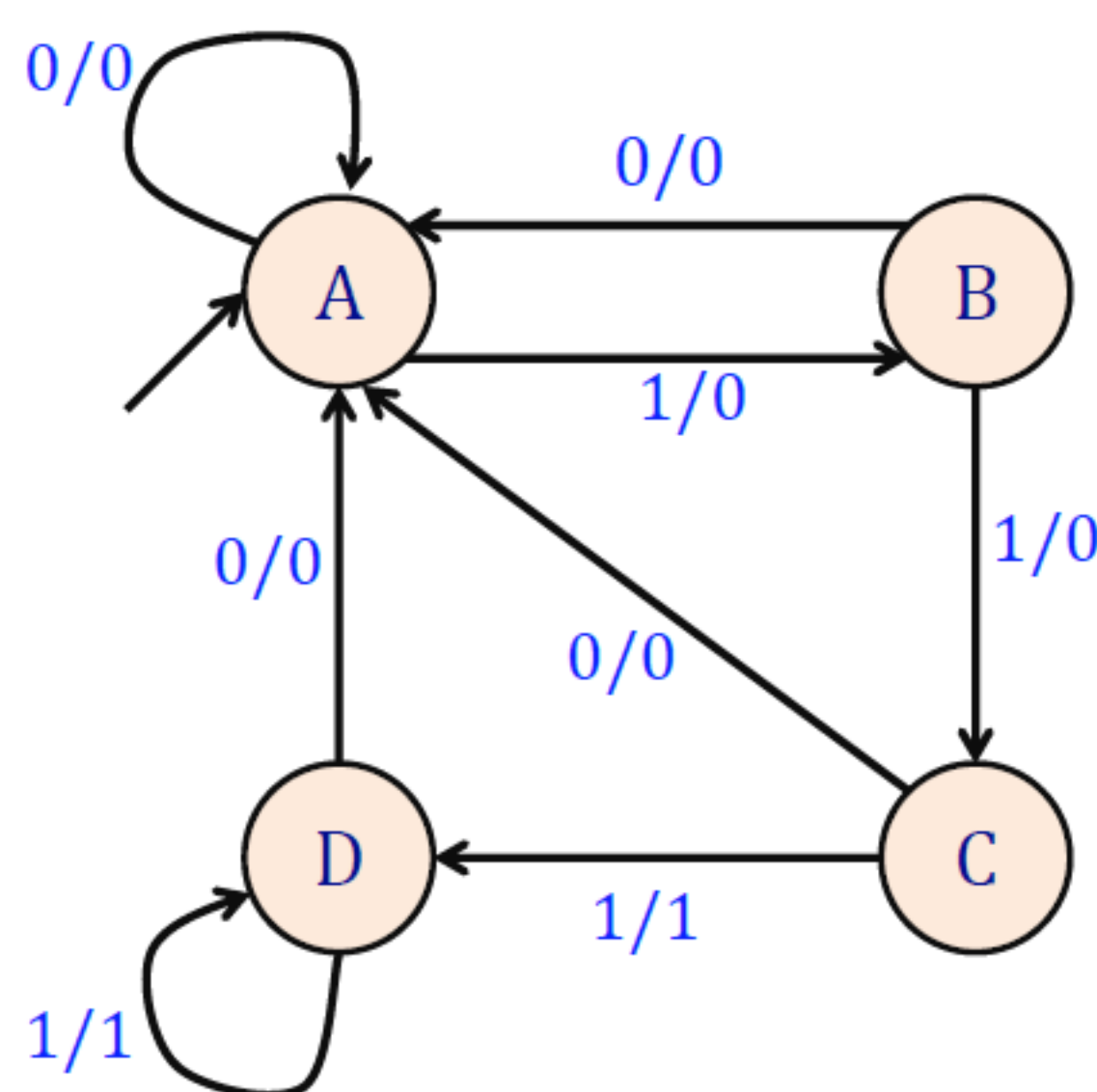
- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.  
Score: 0

Accepted Answers:  
a.

- 3) Consider the following state transition diagram:

1 point



If the machine is in state C, and the input sequence 1 0 0 1 0 is applied, what will be the final state?

- A
- B
- C
- D

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.  
Score: 0

Accepted Answers:  
a.

- 4) Which of the following statements is/are true?
- Serial adder is a Mealy machine.
  - Serial adder is a Moore machine.
  - Serial adder can behave both like a Mealy and a Moore machine in various scenarios.
  - None of these.

1 point

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.  
Score: 0

Accepted Answers:  
a.

- 5) If there are 8 state variables in a FSM, what is the maximum number of states in the state transition diagram?
- 8
  - 16
  - 64
  - 256

1 point

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.  
Score: 0

Accepted Answers:  
d.

- 6) Given a state transition diagram with 50 states, at least how many flip-flops will be required to implement the states?

No, the answer is incorrect.  
Score: 0

Accepted Answers:  
(Type: Numeric) 6

1 point

- 7) Two states A and B of a FSM are said to be equivalent if
- For every input sequence X, the outputs are same but next states can be different.
  - For every input sequence X, the next states are same but outputs can be different.
  - For every input sequence X, the outputs are same and the next states are equivalent.
  - None of these.

1 point

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.  
Score: 0

Accepted Answers:  
c.

- 8) For the given state table as follows, how many states will remain after state minimization?

1 point

PS	NS		Output z
	X=0	X=1	
A	D	C	0
B	F	H	0
C	E	D	1
D	A	E	0
E	C	A	1
F	F	B	1
G	B	H	0
H	C	G	1

- 6
- 7
- 8
- None of these.

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.  
Score: 0

Accepted Answers:  
a.