Unit 7 - Week 5 : Unit 5

Week 5 Assignment 5

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-09-04, 23:59 IST.

1) Suppose you are implementing the CARRY output of a full adder using 2-input AND and OR gates. Assume that the delay of a 2-input AND gate is 3 nanoseconds, and the delay of a 2-input OR gate is 4 nanoseconds. The total propagation delay for generating the CARRY output will be ..... nanoseconds.

1 point

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 11

2) The number of 2-input NAND gates required to implement a 2-input exclusive-OR function is at least

1 point

a. 3
b. 4
c. 5
d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

3) For a full adder, suppose that the propagation delays to generate the SUM and CARRY outputs are 12 nanoseconds and 8 nanoseconds respectively. A 4-bit ripple carry adder is constructed using such full adders. The worst-case propagation delay of the 4-bit adder will be

1 point

a. 32 nanoseconds
b. 36 nanoseconds
c. 48 nanoseconds
d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

4) Which of the following statements are true for a carry lookahead adder?

1 point

a. The carry generate function specifies the condition when a full adder stage can generate a carry irrespective of its carry input.
b. The carry generate function specifies the condition when a full adder stage can generate a carry considering its carry input.
c. The carry propagate function specifies the condition when a carry input can propagate to the carry output in a full adder stage.
d. The cost of the carry lookahead circuit increases rapidly with increase in the number of bits.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.
c.
d.

5) To implement any arbitrary 5-variable function, we need

1 point

a. A 16-to-1 multiplexer and a NOT gate.
b. A 16-to-1 multiplexer and an AND gate.
c. A 16-to-1 multiplexer and an OR gate.
d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.

6) The minimum number of 2-to-1 multiplexers required to build a 16-to-1 multiplexer will be .....

1 point

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 15

7) A 16-bit adder is designed by cascading four 4-bit carry lookahead adder (CLA) modules. If the delay of a 4-bit CLA module (including carry generate and propagate circuits) is 15 nanoseconds, and the delay of an exclusive-OR gate is 7 nanoseconds, the worst-case delay of the adder will be

1 point

a. 60 nanoseconds
b. 67 nanoseconds
c. 88 nanoseconds
d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

8) In addition to a parallel adder in the last stage, what will be the minimum number of carry save adders required to add 10 numbers?

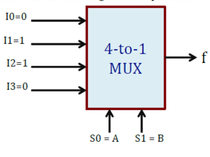
1 point

a. 6
b. 7
c. 8
d. 9

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

9) What function does the following circuit implement?

1 point



a. 2-input exclusive-OR function of A and B.
b. 2-input NAND function of A and B.
c. 2-input OR function of A and B.
d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.

10) For a 7-segment display input, if the output of 1 indicates that a segment will glow, what will be the outputs for displaying the letter 'E'?

1 point

a. A = 1, B = 0, C = 0, D = 0, E = 1, F = 1, G = 1
b. A = 1, B = 0, C = 0, D = 1, E = 1, F = 1, G = 1
c. A = 1, B = 1, C = 0, D = 0, E = 1, F = 0, G = 1
d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.