

Unit 4 - Week 2 : Unit 2

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Week 2 Assignment 2

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-08-21, 23:59 IST.

1) Which of the following statements is/are false with respect to Moore's law? 1 point

- The speed of the transistors shall increase exponentially over the years.
- The number of transistors that can be packed in a chip shall increase linearly over the years.
- The power dissipation of a chip shall increase exponentially over the years.
- All of these.

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

2) The output of a 3-input AND gate will be 0 if 1 point

- All the inputs are 0.
- At least two of the inputs are at 0.
- At least one of the inputs is at 0.
- All of these.

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

3) Consider a 4-input NOR gate with inputs A, B, C and D. What will happen if the input D is permanently set to 0? 1 point

- The output will always be at 1.
- The output will always be at 0.
- It will behave like a 3-input NOR gate with inputs A, B and C.
- None of these.

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.

4) For a 4-input exclusive-OR gate, what will be the outputs corresponding to the inputs 0011 and 1011? 1 point

- 0 and 0
- 0 and 1
- 1 and 0
- 1 and 1

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

5) How many resistances, diodes and transistors will be required to construct a 4-input NAND gate using diode transistor logic? 1 point

- 2, 4 and 1
- 4, 4 and 1
- 4, 2 and 1
- 2, 4 and 4

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.

6) Which of the following are false for MOS transistors? 1 point

- An nMOS transistor conducts when the gate input is at low voltage.
- An nMOS transistor conducts when the gate input is at high voltage.
- A pMOS transistor conducts when the gate input is at low voltage.
- A pMOS transistor conducts when the gate input is at high voltage.

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.
d.

7) A 3-input CMOS OR gate implementation will require 1 point

- 3 nMOS and 3 pMOS transistors
- 3 nMOS and 4 pMOS transistors
- 4 nMOS and 3 pMOS transistors
- None of these

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

8) For constructing a 2-to-1 multiplexer, we require 1 point

- Two transmission gates and a NOT gate
- One transmission gate and a NOT gate
- Four transmission gates and a NOT gate
- None of these

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
a.

9) If the input signals to a Mach Zehnder interferometer are denoted by X and Y, the output at the Cross Port can be represented by 1 point

- X.Y
- XY
- XY'
- X + Y

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.

10) How many memristors will be required to implement a 3-input NOR gate using MAGIC? 1 point

- 3
- 4
- 5
- None of these

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

11) What do you mean by stateful logic design style? 1 point

- The inputs to a logic gate are applied as voltages.
- The inputs to a logic gate are applied as resistive states of memristors.
- Logic operations are mapped to internal states of a gate.
- None of these.

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
b.

12) Consider the material implication operation $A \rightarrow B$. How can you implement the NOT operation? 1 point

- By setting A to 0
- By setting A to 1
- By setting B to 0
- By setting B to 1

- a.
 b.
 c.
 d.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.