

# Unit 14 - Week 12

## Course outline

### How to access the portal

### Week 0 Assignment 0

### Week 1

### Week 2 : Unit 2

### Week 3 : Unit 3

### Week 4 : Unit 4

### Week 5 : Unit 5

### Week 6

### Week 7

### Week 8

### Week 9

### Week 10

### Week 11

### Week 12

Lecture 55 : Testing of Digital Circuits

Lecture 56 : Fault Modeling

Lecture 57 : Test Pattern Generation

Lecture 58 : Design for Testability

Lecture 59 : Built-in Self-Test (Part I)

Lecture 60 : Built-in Self-Test (Part II)

Lecture Materials

Feedback for Week 12

Quiz : Week 12 Assignment 12

### Download Videos

### Text Transcripts

### Detail Solution

### Live Session

## Week 12 Assignment 12

The due date for submitting this assignment has passed.  
As per our records you have not submitted this assignment.

**Due on 2019-10-23, 23:59 IST.**

- 1) Which of the following statements are false?
- Testing is used to guarantee that a circuit/chip is fault free.
  - Verification ensures quality of the design, while testing ensures quality of the manufactured devices.
  - Verification follows testing in the design cycle.
  - All of these.

1 point

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

- a.  
c.

- 2) The total number of multiple stuck-at faults possible in a 4-input AND gate is .....

No, the answer is incorrect.

Score: 0

Accepted Answers:

(Type: Numeric) 242

1 point

- 3) The minimum number of test vectors required to detect all single stuck-at faults in an 11-input exclusive-OR gate is .....

No, the answer is incorrect.

Score: 0

Accepted Answers:

(Type: Numeric) 2

1 point

- 4) The function  $F = A.B.C + D.E$  is realized using two AND gates and one OR gate. The total number of possible single stuck-at faults in the circuit will be .....

No, the answer is incorrect.

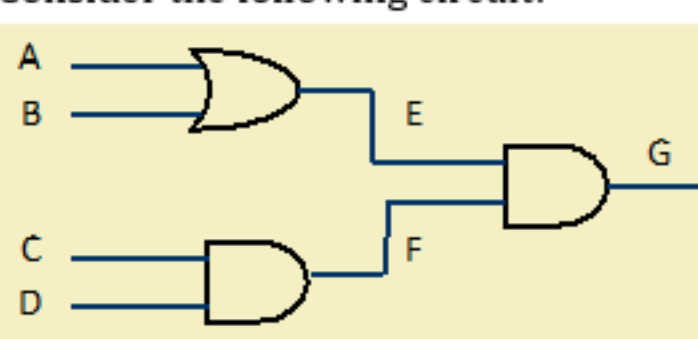
Score: 0

Accepted Answers:

(Type: Numeric) 16

1 point

- 5) Consider the following circuit:



Which of the following test vectors can detect the fault E/0?

- 0111
- 1111
- 0101
- 0011

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

- a.  
b.

- 6) For a 4-input AND gate, which of the following set of faults are equivalent?

- Input lines stuck-at-1 and output stuck-at-0.
- Input lines stuck-at-1 and output stuck-at-1.
- Input lines stuck-at-0 and output stuck-at-0.
- Input lines stuck-at-0 and output stuck-at-1.

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

- c.

1 point

- 7) For a 3-input OR gate with inputs A, B, C and output F, which of the following is/are false with respect to fault dominance?

- F/0 dominates A/0.
- F/0 dominates B/1.
- F/0 dominates C/0.
- B/1 dominates C/1.

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

- b.  
d.

1 point

- 8) The Boolean difference of a function  $F = A'B + B'C + AC'$  with respect to the variable C is given by:

- $A.B + A'.B'$
- $A.B' + A'.B$
- $A + B$
- $A.B'$

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

- a.

1 point

- 9) In a scan path design there are 20 scan flip-flops that are connected in a scan chain. For applying 500 combinational test vectors, how many clock cycles will be required?

No, the answer is incorrect.

Score: 0

Accepted Answers:

(Type: Numeric) 10520

1 point

- 10) For a 24-bit LFSR compacting a 5,000-bit serial bit pattern, the probability of aliasing is approximately given by:

- $1 / 2^{24}$
- $24 / 5000$
- $1 / 2^{5000}$
- None of these

- a.  
 b.  
 c.  
 d.

No, the answer is incorrect.

Score: 0

Accepted Answers:

- a.

1 point