Week 8 Assignment 8

The due date for submitting this assignment has passed. Due on 2019-10-23, 23:59 IST. As per our records you have not submitted this assignment.

1) Suppose that in a MIPS32 based computer, memory locations 500, 504, 508 and 512 (in decimal) contains the data 40, 30, 80 and 10 (in decimal) respectively.

For the following MIPS32 code segment, the final value of R10 will be ............

```
ADDI R5, R0, 35
ADDI R7, R0, 23
LW  R6, 504(R0)
ADD  R5, R5, R7
SUB  R10, R5, R6
```

Hint

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 28

2)
Suppose that in a MIPS32 based computer, memory locations 500, 504, 508 and 512 (in decimal) contains the data 40, 30, 80 and 10 (in decimal) respectively.

After execution of the following MIPS32 code segment, memory location 512 will contain ............

```
ADDI R1, R0, 500
LW R2, 0 (R1)
LW R3, 8 (R1)
ADD R3, R2, R3
SW R3, 12 (R1)
```

3) For the register values \( R2 = 55 \) and \( R6 = 42 \), after execution of the instruction “`SLT R12, R2, R6`”, the contents of R12 will be ........

4) For the register values \( R2 = 55 \) and \( R6 = 42 \), after execution of the instruction “`SGT R12, R2, R6`”, the contents of R12 will be ........

5)
For the instruction encoding as discussed in the lectures, what will be the hexadecimal machine code for the instruction “SUBI R21, R17, 365”?

a. 32'h2e41003d  
b. 32'h2e35016d  
c. 32'h2e35017a  
d. None of these

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
b.

6)  
For the following code segment, what will be the hexadecimal machine code for the BEQZ instruction, assuming the instruction encoding as discussed in the lectures?

<table>
<thead>
<tr>
<th>Loop</th>
<th>ADD</th>
<th>R2, R5, R10</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SUI</td>
<td>R11, R2, 25</td>
</tr>
<tr>
<td></td>
<td>MUL</td>
<td>R3, R2, R1</td>
</tr>
<tr>
<td></td>
<td>ADDI</td>
<td>R7, R0, 12</td>
</tr>
<tr>
<td></td>
<td>BEQZ</td>
<td>R11, Loop</td>
</tr>
</tbody>
</table>

a. 32'h39600005  
b. 32'h3960ffff  
c. 32'h3960fff9  
d. None of these

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
d.

7)  
The decimal number -5 is represented in 4-bit binary 2's complement notation. It is sign extended to 24 bits. The sign extended value in hexadecimal will be

a. FFFFF5  
b. FFFFFF  
c. 800000B  
d. None of these

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
a.
8) Why is the **HALTED** signal required in the Verilog implementation of the processor as discussed in the lecture?

- a. It is used for an external device to halt the processor.
- b. It is used by the processor to halt any external device.
- c. It is used to indicate that the processor has started its execution.
- d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers: 

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