Week 7 Assignment 7

The due date for submitting this assignment has passed. Due on 2019-10-16, 23:59 IST. As per our records you have not submitted this assignment.

1) What does the declaration “reg [16:0] mem[15:0]” indicate?
   a. A 2-dimensional array with 17 rows and 16 columns, where every element is a single bit.
   b. An array of 16 elements, each containing 17 bits.
   c. An array of 17 words, each word consisting of 16 bits.
   d. None of these.

   - a.
   - b.
   - c.
   - d.

No, the answer is incorrect.
Score: 0
Accepted Answers: b.

2)
What does the declaration "reg mem[16:0][15:0]" indicate?

a. A 2-dimensional array with 17 rows and 16 columns, where every element is a single bit.
b. An array of 16 elements, each containing 17 bits.
c. An array of 17 words, each word consisting of 16 bits.
d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.

Which of the following is/are false for modeling register banks in Verilog?

a. Register read operation can be carried out using blocking assignment.
b. Register write operation can be carried out using non-blocking statement in synchronism with the clock.
c. A register read and register write operation can be carried out simultaneously.
d. A register bank can be defined only on "reg" type variables.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

Some computation is carried out using a 6-stage pipeline. For processing a large number of data items that are arriving in synchronism with a clock, the maximum speedup that can be obtained is upper bounded by:

a. 5
b. 6
c. 64
d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.
5) Consider a pipelined processor where the inter-stage pipeline registers are assumed to have a delay of 1 nanosecond. Which of the following pipelines will have the highest clock frequency?
   a. 4-stage pipeline with stage delays 3, 5, 4 and 2 nanoseconds
   b. 4-stage pipeline with stage delays 3, 2.5, 3.5, and 3.5 nanoseconds
   c. 5-stage pipeline with stage delays 1, 2.5, 0.6, and 2 nanoseconds
   d. 5-stage pipeline with stage delays 2.5, 3.5, 1.3, 2 and 4.1 nanoseconds

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   b.

6) The stage delays in a 4-stage pipeline are 70, 45, 40 and 55 nanoseconds. The first stage is replaced with a functionally equivalent design involving two stages with respective delays of 40 and 35 nanoseconds, and the fourth stage is replaced by two stages with delays of 32 and 34 nanoseconds. Ignoring the delays of inter-stage registers, the execution time for 1000 data items decreases by .......... microseconds.

   Hint
   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   (Type: Range) 24.9,25.0

7) Why is it sometimes required to forward some value from one pipeline stage to the next without any change?
   a. The stage is a dummy stage not doing any computation.
   b. The value is required by a subsequent stage of the pipeline.
   c. It helps in reducing the delays in pipeline implementation.
   d. None of these.

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   b.
c.

8) What function does the following switch-level model realize?

```verilog
module some_gate (in1, in2, out);
  input in1, in2;  output out;
  supply1 vplus;  supply0 vgnd;
  wire t;
  pmos (t, vplus, in1);
  pmos (out, t, in2);
  nmos (out, vgnd, in1);
  nmos (out, vgnd, in2);
endmodule
```

a. NAND
b. Exclusive OR
c. AND
d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

9) Suppose we are constructing a 16-to-1 multiplexer using cmos switches. In addition to four NOT gates, the number of cmos switches required will be .......... (Assume the design conventions discussed in Lecture 36).

Hint

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 64

10)
Which of the following statements is/are false?

a. A `tranif0` switch allows bidirectional flow of data between the two end terminals when the control signal is 0.

b. A `tranif0` switch allows bidirectional flow of data between the two end terminals when the control signal is 1.

c. A `tranif1` switch allows bidirectional flow of data between the two end terminals when the control signal is 0.

d. A `tranif1` switch allows bidirectional flow of data between the two end terminals when the control signal is 1.

No, the answer is incorrect.
Score: 0
Accepted Answers:
- b.
- c.