Unit 7 - Week 5

Week 5 Assignment 5

The due date for submitting this assignment has passed. Due on 2019-10-02, 23:59 IST.

As per our records you have not submitted this assignment.

1) Which of the following is/are true for a test bench?
   a. A test bench is executed only once during simulation.
   b. The input ports of the module being tested have to be declared as outputs/registers in the test bench.
   c. A test bench is synthesized once during synthesis.
   d. We cannot use “always” procedural block inside a test bench.

   □ a.  
   □ b.  
   □ c.  
   □ d.  

No, the answer is incorrect.

Score: 0

Accepted Answers:
   a.
   b.

2)
Which of the following is/are false for an "initial" block?

a. It can be used to verify whether a given module is synthesizable.

b. "wire" type variables can be assigned inside the block.

c. The right hand side of the assignments can have both net and register type variables.

d. All of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:

Which of the following statements are true?

a. The $display command prints the values of the text / variables as soon as it is executed.

b. The $display command prints the values of the text / variables when one or more of the specified variables changes value.

c. The $monitor command prints the values of the text / variables as soon as it is executed.

d. The $monitor command prints the values of the text / variables when one or more of the specified variables changes value.

No, the answer is incorrect.
Score: 0
Accepted Answers:

4) What happens when the first parameter of the $dumpvars function is specified as 1?

a. Only the listed variables will be dumped.

b. Only the listed variables and variables of listed modules will be dumped.

c. All variables in the top-level module will be dumped.

d. None of the above.

No, the answer is incorrect.
Score: 0
Accepted Answers:
No, the answer is incorrect.
Score: 0
Accepted Answers: 
b.

5) What does the following code segment do?

```verilog
reg a, b, c, d, e; integer count;
for (count=0; count<32; count=count+1)
begin
  {a,b,c,d,e} = count;
end
```

a. Assign the value of “count” to all the five variables a, b, c, d, e in the loop.
b. Assign all possible 5-bit binary patterns to the variables a, b, c, d, e.
c. The five most significant bits of “count” are assigned to the variables a, b, c, d, e.
d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers: 
b.

6) The time period of the clock (clk) generated by the following code segment will be ....... time units.

```verilog
initial
  #15 clk = 1'b0;
always
  #12 clk = ~clk;
```

No, the answer is incorrect.
Score: 0
Accepted Answers: 
(Type: Numeric) 24

7)
The duty cycle of a periodic digital signal is defined as the ON period divided by the total time period. For generating a signal "clk" with duty cycle 0.25, what must be the value of X?

```verilog
initial
    clk = 1'b0;
always
    forever begin
        #3 clk = 1'b0;
        #X clk = 1'b1;
        #4 clk = 1'b0;
    end
```

a. 7  
b. 8  
c. 9  
d. 10

- a.  
- b.  
- c.  
- d.  

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
- c.

8) Which of the following statements is/are true?

- a. Moore machine is more general than Mealy machine.
- b. The number of states in a Mealy machine must be finite.
- c. The number of states in a Moore machine must be finite.
- d. A Moore machine can be realized using a combinational circuit.

- a.  
- b.  
- c.  
- d.  

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
- b.  
- c.
The number of flip-flops will be realized by the following code segment will be:

```verilog
module myfsm (clk, lamp);
    input clk;
    output reg [3:0] lamp;
    parameter S0=0, S1=1, S2=2, S3=3;
    reg [0:1] state;
    always @(posedge clk)
        case (state)
            S0: begin
                lamp <= 4'b1100; state <= S1;
                end
            S1: begin
                lamp <= 4'b0110; state <= S2;
                end
            S2: begin
                lamp <= 4'b0011; state <= S3;
                end
            S3: begin
                lamp <= 4'b1001; state <= S0;
                end
        endcase
    endmodule
```

a. 4
b. 6
c. 8
d. 16

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.
The number of flip-flops will be realized by the following code segment will be:

```verilog
module my fsm (clk, lamp);
  input clk;
  output reg [3:0] lamp;
  parameter S0=0, S1=1, S2=2, S3=3;
  reg [0:1] state;
  always @(posedge clk)
    case (state)
      S0: state <= S1;
      S1: state <= S2;
      S2: state <= S3;
      S3: state <= S0;
    endcase
  always @(state)
    case (state)
      S0: lamp = 4'b1100;
      S1: lamp = 4'b0110;
      S2: lamp = 4'b0011;
      S3: lamp = 4'b1001;
    endcase
endmodule
```

a. 2
b. 4
c. 6
d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.