Week 3 Assignment 3

The due date for submitting this assignment has passed. Due on 2019-09-18, 23:59 IST.
As per our records you have not submitted this assignment.

1) Which of the following statements is/are true?

- a. The "assign" statement implements continuous assignment between the expression specified on the right-hand side and a "net" type variable specified on the left-hand side.
- b. The "assign" statement implements continuous assignment between the expression specified on the right-hand side and a "reg" type variable specified on the left-hand side.
- c. The "assign" statement can be used to model a latch, which is a sequential circuit.
- d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
- a.
- c.
2) Which of the following are true for the following code segment?

```verilog
input [15:0] a;
input [5:2] b;
input sel;
output f;
assign f = sel ? a[b] : 'b0;
```

a. One 32-to-1 and one 2-to-1 multiplexers will be generated.
b. Only one 16-to-1 multiplexer will be generated.
c. One 16-to-1 and one 2-to-1 multiplexers will be generated.
d. None of these.

- No, the answer is incorrect.
- Score: 0
- Accepted Answers: c.

3) Which of the following constructs will be generating a multiplexer, where “a”, “b” and “c” are variables?

```verilog
a. assign a = b[c];
b. assign b[c] = a;
c. assign a = (b) ? c : ~c;
d. assign a = b & c
```

- No, the answer is incorrect.
- Score: 0
- Accepted Answers: a.

4) What does the following code segment implement?

```verilog
assign d = ~(c | b);
assign c = ~(a | d);
```

b. A 2-bit shift-register.
c. Two NOR gates connected in cascade.
d. A 2-bit comparator.

- a.
5) What is the purpose of the “initial” procedural block in Verilog test benches?
   a. It is used to specify a procedural block that is executed only once.
   b. It can be used to specify a procedural block for synthesis.
   c. Every time an “always” block is executed, variables are initialized as specified in the “initial” block.
   d. If there are multiple “initial” blocks in a module, they are executed one by one in sequence.

   No, the answer is incorrect.
   Score: 0
   Accepted Answers: a.

6) The following code segment generates a periodic clock signal “clk” with time period:
   ```verilog
   initial clk = 1'b1;
   always #10 clk = ~clk;
   ```
   a. 10
   b. 20
   c. 30
   d. None of these

   No, the answer is incorrect.
   Score: 0
   Accepted Answers: b.
If "clk" and "clear" are two inputs of a counter module, which of the following event expressions must be used if we want to implement asynchronous clear (assuming "clear" is active low, active high edge of "clk" signal is used for counting, and single "always" block is used for the implementation)?

a. always @(posedge clk)
b. always @(negedge clear)
c. always @(posedge clk or negedge clear)
d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

8) 1 point

Which of the following is true for the following module?

```verilog
module mydesign (a, b);
  input [1:0] b;
  output reg a;
  always @(b)
  begin
    if (b == 2'b00) a = 1'b0;
    else if (b == 2'b11) a = 1'b0;
    else a = 1'b1;
  end
endmodule
```

a. A combinational circuit implementing a XOR function will be generated.
b. A combinational circuit implementing an AND function will be generated.
c. A latch will be generated for the output "a".
d. The synthesis tool will give an error.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.
Which of the following is true for the “repeat” loop?

a. It can be used to iterate a block until a specified condition is true.
b. It can be used to iterate a block indefinitely.
c. It can be used to repeat execution of the block exactly two times.
d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

What does the construct “#5” indicate in simulation?

a. It specifies that the unit of delay is 5 nanoseconds.
b. It specifies a delay of 5 time units before executing the next statement.
c. It schedules the execution of the next statement at time 5.
d. It pauses execution of the statements that follow after time 5.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

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