Week 2 Assignment 2

The due date for submitting this assignment has passed. Due on 2019-09-11, 23:59 IST. As per our records you have not submitted this assignment.

1) Which of the following statements is/are false for Verilog modules?
   a. A module can contain one or more definitions of other modules.
   b. If a module X is instantiated 4 times within another module Y, only one copy of X is created, which is linked 4 times.
   c. A module can be instantiated within another module any number of times.
   d. If a module X is instantiated 4 times within another module, 4 copies of X are created.

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   a.
   b.

2)
What does the statement “assign f = (a | b) & (c | d)” signify?
   a. A gate level netlist consisting of two OR gates, and one AND gate.
   b. A behavioral description of the function f.
   c. A structural description of the function f.
   d. None of these.

   a. 
   b. 
   c. 
   d. 

No, the answer is incorrect.
Score: 0
Accepted Answers:
b. 

3) Which of the following is/are true for register type variables?
   a. They always map to a hardware register after synthesis.
   b. They can be used in an expression on the RHS of an “assign” statement.
   c. They may also be used to model a combinational circuit.
   d. None of these.

   a. 
   b. 
   c. 
   d. 

For the following Verilog code segment, what will be the number of bits in “sum” as deduced during synthesis?

```verilog
wire [6:0] data1, data2;
reg [7:0] dummy;
integer sum;
sum = (data1 + data2) + dummy;
```

a. 7
b. 8

No, the answer is incorrect.
Score: 0
Accepted Answers:
b. 
c. 

d. None of these

Week 3
Week 4
Week 5
No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

5) For the following Verilog code segment, if the initial value of IR is 2D00 023A (in hexadecimal), what will be the value of “memaddr” in decimal?

```
wire [31:0] IR;
wire [7:0] opcode;
wire [23:0] address;
wire [23:0] memaddr;
assign opcode = IR[31:24];
assign address = IR[23:0];
assign memaddr = address + 100;
```

a. 685
b. 670
c. 723
d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

6)
Consider the following Verilog module.

```verilog
module ALU (data1, data2, cond, result);
    input [7:0] data1, data2;
    input [2:0] cond;
    output reg [7:0] result;
    always @(data1 or data2 or cond)
        begin
            if (cond == 3'b000) result = data1;
            else if (cond == 3'b001) result = data2;
            else if (cond == 3'b010) result = data1 + data2;
            else if (cond == 3'b011) result = data1 - data2;
            else if (cond == 3'b101) result = data1 & data2;
            else if (cond == 3'b110) result = data1 | data2;
            else if (cond == 3'b111) result = 0;
        end
    endmodule
```

What will happen when the module is synthesized?

a. A combinational circuit will be generated.
b. A sequential circuit with storage elements will be generated.
c. If the synthesizer supports adder and subtractor blocks, a combinational circuit will be generated.
d. None of these.

- [ ] a.
- [ ] b.
- [ ] c.
- [ ] d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
- b.

7) Consider the following Verilog code segment:

```verilog
wire [5:0] A, B;
wire C;
assign C = ~A;
```

If the values of A and B are 5'b10011 and 5'b011110 respectively, what will be the value of {A[3:1], 2(C), B[2:0]}?

a. 00100110
b. 00111110
c. 01111110
d. None of these

- [ ] a.
- [ ] b.
- [ ] c.
- [ ] d.

No, the answer is incorrect.
Score: 0
8) When does the $monitor statement in a Verilog test bench print the specified values?
   a. At the start of the simulation.
   b. When the $monitor statement is first encountered.
   c. Whenever the value of any of the specified variables change.
   d. None of the above.

   Accepted Answers:
   b.

   1 point
   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   c.

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