Week 1 Assignment 1
The due date for submitting this assignment has passed. Due on 2019-09-11, 23:59 IST.
As per our records you have not submitted this assignment.

1) **What does Moore’s law specify?**
   - a. The number of transistors in a VLSI chip will increase exponentially with time.
   - b. The power consumption in a VLSI chip will increase linearly with time.
   - c. The clock speed of a VLSI chip will increase exponentially with time.
   - d. None of these.

   - a.
   - b.
   - c.
   - d.

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   a.

2) **Which of the following does not represent a behavioral representation for the function f = \( A \cdot B + B \cdot C + C \cdot A \)?**
   - a. A truth table of the function \( f \)
   - b. The Verilog specification: assign \( f = (A \& B) \mid (B \& C) \mid (C \& A); \)
   - c. A netlist consisting of three 2-input AND and one 3-input OR gate
   - d. None of these

https://onlinecourses.nptel.ac.in/noc19_cs72/unit?unit=5&assessment=79
Which of the following functional descriptions can be realized by a single 4-input LUT in a typical FPGA?

- a. \( F = A'B'C + B'C' \)
- b. \( F = (A.B + A'B') \cdot (C.D' + C'.D) \)
- c. \( F = A.B.C + E'.D.E \)
- d. All of these

No, the answer is incorrect.
Score: 0
Accepted Answers: c.

4) **1 point**

For which design style, the following statement is true?

"The fabrication cost of a chip is \( C = C1 + C2 \), where \( C1 \) represents a cost that is shared among several customers, while \( C2 \) represents a cost that is to be separately borne by every customer."

- a. Gate array
- b. FPGA
- c. Standard cell
- d. Full custom

No, the answer is incorrect.
Score: 0
Accepted Answers: a.
Which of the following are true for standard cell based design?
   a. The heights of the cells are fixed but the widths can be different.
   b. The number of cells must be equally distributed among the rows.
   c. Feed-through cells can be inserted to improve routability.
   d. It requires more design effort as compared to full custom design.

☐ a.
☐ b.
☐ c.
☐ d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
   a.
   c.

6) Which of the following results in shortest design turnaround time?
   a. Full custom design
   b. Standard cell design
   c. FPGA based design
   d. Gate array design

☐ a.
☐ b.
☐ c.
☐ d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
   c.

7) Which of the following are examples of structural design representation?
   a. A netlist of functional blocks.
   b. A netlist of gates and flip-flops.
   c. A truth table description.
   d. All of these.

☐ a.
☐ b.
☐ c.
☐ d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
   a.
8) Which of the following statements is/are true?

- a. A test bench is required when we want to verify a design through simulation.
- b. A test bench is also synthesized along with the main module.
- c. When we map the design to a FPGA or ASIC, we do not need a test bench.
- d. Simulation means generation of a gate level netlist from a behavioral specification.

No, the answer is incorrect.
Score: 0
Accepted Answers: a, c.

9) What function do the following Verilog module implement?

```verilog
module guess (f, a, b, c);
    input a, b, c;
    output f;
    wire t1, t2;
    nand #1 G1 (t1, a, b);
    or #1 G2 (t2, b, c);
    nor #1 G3 (f, t1, t2);
endmodule
```

- a. \( f = a' \cdot c \)
- b. \( f = a \cdot c' \)
- c. \( f = (a + c)' \)
- d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers: d.
What function do the following Verilog module implement?

```
module guess (f, a, b, c);
    input a, b, c; output f;
    wire t;
    assign t = (a ^ b);
    assign f = t & c;
endmodule
```

a. \( f = a'.b.c + a.b'.c \)
b. \( f = a'.b.c + a.b.c' \)
c. \( f = a'.c + a'.b.c' \)
d. None of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.