Assignment 6

The due date for submitting this assignment has passed. Due on 2019-03-13, 23:59 IST.
As per our records you have not submitted this assignment.

1) Which of the following statement is/are correct in regards to memory?
a. The faster, smaller memory are always closer to the processor
b. The memory that is farthest away from the processor is the costliest.
c. As we move away from the processor, speed increases.
d. None of the above

☐ a.  
☐ b.  
☐ c.  
☐ d.  

No, the answer is incorrect.
Score: 0
Accepted Answers:
a.

2) Which of the following statements are false?
a. Temporal locality arises because of loops in a program.
b. Memory speedup can be achieved through the principle of locality of reference
c. Spatial locality arises because of sequential instruction execution.
d. None of these.

☐ a.  
☐ b.  
☐ c.  
☐ d.  

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.
4) Assume that we have a computer with a 2-level memory hierarchy consisting of a cache memory $L_1$ and the main memory $L_2$. Suppose that the cache is 8 times faster than main memory, and the cache has a hit ratio of 90%. The speedup attained by using a cache is _________ (up to one decimal point).

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 9.55, 9.65

5) In a two-level cache system, the hit time of the first cache $L_1$ is 20 nsec and that of $L_2$ is 40 nsec. If the hit rate of $L_1$ is 80% and that of $L_2$ is 90%, and the miss penalty on a cache miss is 10 nsec. The average memory access time is _________ nsec.

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 23.4

6) Which of the following statements is/are false?
   a. Direct mapping technique is the easiest way of mapping a cache.
   b. The set associative mapping requires associative memory for implementation.
   c. In set-associative mapping, a main memory block can be placed in any of the blocks in the selected set.
   d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

7) Consider a direct-mapped cache of size 1 Mbyte and a 32 bit addresses. If the block size is 512 byte. The number of tag bits is ________.
No, the answer is incorrect.
Score: 0

Accepted Answers:
(Type: Numeric) 12

8) Which of the following statements is false for cache misses?
   a. Compulsory miss can be reduced by increasing the cache block size.
   b. Capacity miss can be reduced by increasing the total size of the cache.
   c. Conflict miss can be reduced by decreasing the value of cache associativity.
   d. Compulsory miss can be reduced by prefetching cache blocks.

No, the answer is incorrect.
Score: 0

Accepted Answers:
c.

9) Which of the following statement is false?
   a. Cache miss rate can be reduced by using larger block size.
   b. Cache miss rate can be reduced by using larger cache size.
   c. Cache miss rate can be reduced by increasing the cache associativity.
   d. All of these.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.

10) Which of the following statement is false?
    a. Miss penalty increases with increase in block size.
    b. Miss penalty can be reduced by using a multi-level cache.
    c. Capacity misses can be reduced by increasing cache size.
    d. None of these.

No, the answer is incorrect.
Score: 0

Accepted Answers:
d.