Assignment 4

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2019-02-27, 23:59 IST.

1) Which of the following statement is/are correct?

- a. MIPS instructions are 32 bits long.
- b. All instructions are stored in memory with address having the last two bits 00.
- c. Program Counter is decremented to 4 to point to the next instruction
- d. All of these

No, the answer is incorrect.
Score: 0
Accepted Answers:
- a. MIPS instructions are 32 bits long.
- b. All instructions are stored in memory with address having the last two bits 00.

2) The correct sequence in Fetch-Execute cycle is:

- a. Decode, Fetch, Execute
- b. Fetch, Execute, Decode
- c. Fetch, Decode, Execute
- d. None of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
- c. Fetch, Decode, Execute

3) The minimum number of time steps needed to execute the instruction “ADD R1, R2” (Meaning: R1 ← R1 + R2) in a single bus architecture will be ______. Consider the single bus architecture provided in the slides for the calculation.
4) Which instruction does the following set of micro-operations refer to?

<table>
<thead>
<tr>
<th>Steps</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCout, MARin, Read, Select4, Add, Zin</td>
</tr>
<tr>
<td>2</td>
<td>Zout, PCin, Yin, WMFC</td>
</tr>
<tr>
<td>3</td>
<td>MDRout, IRin</td>
</tr>
<tr>
<td>4</td>
<td>R1out, Yin</td>
</tr>
<tr>
<td>5</td>
<td>R2out, SelectY, Add, Zin</td>
</tr>
<tr>
<td>6</td>
<td>Zout, R1in, End</td>
</tr>
</tbody>
</table>

- a. ADD R2, R1
- b. ADD R1, R2
- c. MOVE R1, R2
- d. MOVE R2, R1

No, the answer is incorrect.
Score: 0
Accepted Answers:
- b. ADD R1, R2

5) The Instruction Register (IR)

- a. Holds the memory address of the next instruction.
- b. Holds the memory address of the current instruction.
- c. Holds the encoded instruction that is currently being executed or decoded.
- d. Holds the executed or decoded instruction.

No, the answer is incorrect.
Score: 0
Accepted Answers:
- c. Holds the encoded instruction that is currently being executed or decoded.

6) Which of the following statements are true for vertical micro-instruction encoding?

- a. If there are $2^k$ control signals, every control word stored in control memory (CM) consists of $k$ bits, one bit for every control signal.
- b. Sequential activation of at most one control signal in a single time step.
- c. Low cost of implementation.
- d. None of these.

No, the answer is incorrect.
Score: 0
Accepted Answers:
- a. If there are $2^k$ control signals, every control word stored in control memory (CM) consists of $k$ bits, or bit for every control signal.
- b. Sequential activation of at most one control signal in a single time step.
- c. Low cost of implementation.

7) Which of the following statements is/are false?

- a. Diagonal micro-instructions encoding requires multiple decoders.
- b. In vertical micro-instructions encoding, more than one control signals cannot be activated at a time.
- c. Horizontal micro-instructions encoding has a lower cost of implementation.
- d. None of these.

No, the answer is incorrect.
8) Which of the following is true for MIPS32 register bank?
   a. There is one read port and one write port.
   b. There is one read port and two write ports.
   c. There are two read ports and one write port.
   d. None of these.
   Score: 0
   Accepted Answers:
   c. Horizontal micro-instructions encoding has a lower cost of implementation.

9) Which of the following is the correct MIPS32 instruction cycle?
   a. Instruction Fetch, Instruction Decode, Execute, Memory Access, Write Back
   b. Instruction Decode, Instruction Fetch, Execute, Memory Access, Write Back
   c. Instruction Fetch, Instruction Decode, Execute, Write Back, Memory Access
   d. Instruction Decode, Instruction Fetch, Execute, Write Back, Memory Access
   Score: 0
   Accepted Answers:
   a. Instruction Fetch, Instruction Decode, Execute, Memory Access, Write Back

10) Which of the following is not true for a branch instruction in MIPS32?
    a. The target address is computed in ID stage.
    b. The new PC value is loaded in the MEM stage.
    c. The branch condition is computed in EX stage.
    d. The WB stage is not required.
    Score: 0
    Accepted Answers:
    a. The target address is computed in ID stage.