Assignment 10

The due date for submitting this assignment has passed. Due on 2019-04-10, 23:59 IST.
As per our records you have not submitted this assignment.

1) Which of the following are true for DMA data transfer?
   a. Not suitable for large blocks of data transfer.
   b. DATA transfer requires continuous CPU intervention.
   c. It performs asynchronous data transfer.
   d. No instruction execution is required during data transfer.

   □ a
   □ b
   □ c
   □ d

   No, the answer is incorrect.
   Score: 0
   Accepted Answers: d

2) Assume that 10 instructions are required for each word transfer in programmed I/O mode of transfer, and CPI of the system running at 2GHz clock is 3. The word transfer will be _________ M words/sec. (Assume 1M = 1000K)

   _________ M words/sec

   Hint

   No, the answer is incorrect.
   Score: 0
   Accepted Answers: (Type: Range) 66.00, 67.00

3) Suppose the rotational speed of a disk is 30,000 rpm and 150 clusters of data are passed

   _________ M words/sec
4) Assume that a pipelined processor having 4 stages fetch, decode, execute, and write back with each stage operation is carried out in one machine cycle. The processor also has interrupt and DMA facilities available. Which of the following statements is/are true regarding interrupt and DMA acknowledgement?

a. Interrupt breakpoints can be at the end of any machine cycle.

b. DMA requests can be acknowledged at the end of fetch stage.

c. Interrupt requests can only be acknowledged at the end of execution stage.

d. DMA requests can only be acknowledged at the end of write back stage.

5) The size of the word count register of a DMA controller is 13 bits. The processor needs to transfer a file of 16 Mbytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get control the system bus from the processor to transfer the file from disk to main memory is ................. (Assume 1M = 1024K).

6)
Which of the following statements are false?

a. DMA controller is initialized by the I/O device for number of bytes to be transferred.
b. The DMA controller sends DMA-ACK signal to I/O device after getting DMA-RX signal form the I/O device.
c. The DMA transfer begins after CPU relinquishes the bus control.
d. CPU provides information about number of bytes to be transferred and memory address to DMA controller.

No, the answer is incorrect.
Score: 0
Accepted Answers:
a  
b

c

Hint

No, the answer is incorrect.
Score: 0
Accepted Answers:

7) For interfacing a matrix keyboard with 256 keys, the minimum number of port lines required for interfacing is ________. Assume that each of the row/column junctions has a key connected.

(Type: Numeric) 32

8) If we apply bit stuffing on the bit stream 1110111111111111011011011111100, output bit stream will be:

a. 11101111110111111011011111100
b. 111011111111111101101101100

32

c. 1110011111111111011001111100

d. 11101111110111110101101111100

No, the answer is incorrect.
Score: 0
Accepted Answers:
d

9)
Which of the following statements are false?

a. USB Type-A plug can be inserted into downstream port on a USB host.
b. USB Type-B plug can be inserted into a downstream port of a device.
c. The supported data transfer rate of USB 2.0 is up to 10 Mbps.
d. The main objective of USB bus is to simplify connection and software configuration of connected device.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b
c

A DMA controller transfers 64-bit words from an input device to memory in one cycle using cycle stealing. The input device transmits data at a rate of 12 Kbytes second. The CPU is fetching and executing instructions at an average rate of 150, instructions per second (assume 64-bit instructions). The CPU will be slowed down because of the DMA transfer by ________ percent. (Assume 1K = 1024)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 1.0-1.1

1 point