Week 4 Assignment 4

1. For a channel routing problem, a 2-track layout from a net in the horizontal channel indicates that:
   a. There is a pin blocked on the top boundary and there is a pin blocked on the bottom boundary on one of the channels.
   b. The horizontal spaces of the two tracks are 3 and 3.5, respectively.
   c. The horizontal spaces of the two tracks are 2 and 2.5, respectively.
   d. None of the above.

2. For a channel routing problem, an edge between a net 1 and a net 2 in the horizontal channel indicates that:
   a. There is a pin blocked on the top boundary and there is a pin blocked on the bottom boundary on one of the channels.
   b. The horizontal spaces of the two tracks are 3 and 3.5, respectively.
   c. The horizontal spaces of the two tracks are 2 and 2.5, respectively.
   d. None of the above.

3. In channel routing, under what conditions structures such as this net 1 and an empty net cannot be assigned to separate tracks?
   a. The two edges are directed from a to b.
   b. There is a directed edge from a to b in the vertical constrained graph.
   c. There is a directed edge from b to a in the vertical constrained graph.
   d. None of the above.

4. Consider a channel with TOP = (T1, T2, T3, T4) and BOTTOM = (B1, B2, B3, B4), which of the following is the possible routing of the channel?
   a. T1 and T2
   b. T2 and T3
   c. T3 and T4
   d. None of the above

5. Which of the following channel routing algorithms can handle cycles in the channel?
   a. Earliest-fit channel routing algorithm
   b. First-fit channel routing algorithm
   c. Strict-first-fit channel routing algorithm
   d. None of the above

6. With respect to the direction of a clock signal, what do you mean by clock skew?
   a. Variations in the time to set and reset of a flip-flop, or channel signal at a symmetric.
   b. Variations in the delay between clock pulses of the same clock node.
   c. The width of the clock is insufficient to drive the logical loads.
   d. None of the above.

7. The basic solution to clock routing is which of the following? Which of the following is the correct answer?
   a. Ensure a uniformity between clock delays on either the horizontal or vertical graph.
   b. Crossover connections in the channel.
   c. The routing of the clock must be at the bottom of the channel.
   d. None of the above.

8. Which of the following statements is false?
   a. Logic and clock nets are directly related to clock skew and jitter.
   b. Setup and hold times are directly related to the electrical characteristics of the flip-flops.
   c. Setup time relates to clock skew and jitter, while hold time relates to the characteristics of the flip-flops.
   d. None of the above.

9. The dynamic power dissipation of the clock distribution network is directly proportional to:
   a. The number of levels
   b. The number of clock nodes
   c. The number of loads
   d. None of the above.