Week 2 Assignment 2

Due on 2020-08-19, 20:00 ET

1. In the worst case, the run time of the algorithm for partitioning becomes as:
   a. Linear to the number of circuit nodes.
   b. Square of the number of circuit nodes.
   c. Cubed of the number of circuit nodes.
   d. Exponential of the number of circuit nodes.

2. Consider a rectangle for blocks 1 and 7 with their centers located in the coordinates (11, 8) and (20, 15) respectively. There are 3 lines that connect the two blocks. What will be the x-width distances between them if?
   a. 2
   b. 5
   c. 10
   d. None of these.

3. Which of the following is a neuron?
   a. A polarized transistors partition graph.
   b. A polarized transistors partition graph.
   c. A neuron graph contains a neuron.
   d. If the partition graph does not contain any complex triangle, it is not possible to find a neuron.

4. Draw the following circuit:
   a. A triode bipolar junction.
   b. A triode p-n-n+.
   c. A trio.
   d. A circuit realizing the function $F = A + B + C + D$.

5. Consider a 4-terminal net with terminal coordinates (10, 5), (20, 5), (20, 10), and (10, 10) respectively. The estimated length of the net using the complete graph topology will be:
   a. 10
   b. 15
   c. 20
   d. None of these.

6. Which of the following statements are true for an algorithm based on computational solving?
   a. The cost of solving becomes exponentially lower as the number of solutions increases.
   b. The probability of achieving a unique solution decreases as the number of solutions increases.
   c. A linear time algorithm guarantees the generation of an optimal solution.
   d. All of these.

7. Consider the following placement problem applied to a 40-pin diode that has five blocks A, B, C, D, and E with their centers located in the grid coordinates (0,1), (2,1), (1,3) and (3,1) respectively. A 40-pin diode is required to be placed, where each cell in the placement includes a minimum of 1 Syracuse block. The interference target distance of 4.25 units was optional, but was required. What will be the x-width distance between?
   a. 2
   b. 3
   c. 4
   d. 5

8. With respect to modeling interconnects during layout, which of the following topologies are used?
   a. Complete graph
   b. Minimum spanning tree
   c. Rectangular lattice tree
   d. Linear graphs