Week 1 Assignment 1

Due on 2020-02-18, 23:59:59.

Which of the following represents the behavioral description of a function? Select all that apply:

A. 6. x + y = z
B. 7. z = x + y
C. 8. (x, y, z) = (x, y, z)
D. 9. x = 2
E. 10. z = y + x

Which of the following functions can be realized by a single 4-input OR gate? Select all that apply:

A. 11. f(x, y, z, w) = x
B. 12. f(x, y, z, w) = x + y
C. 13. f(x, y, z, w) = x + w
D. 14. f(x, y, z, w) = w + z
E. 15. f(x, y, z, w) = x + y + z

Consider a copper wire, fabrication facility, where the chips designed by three technicians, 1, 2 and 3 are being fabricated. It is known that technician 1 completes 200 units by 10:00 AM, 200 units by 12:00 PM and 200 units by 2:00 PM. Technician 2 completes 200 units by 1:00 PM and 200 units by 3:00 PM. Technician 3 completes 200 units by 2:00 PM and 200 units by 4:00 PM. How many units can be completed by technician 2 by 3:00 PM?

A. 16. 200
B. 17. 400
C. 18. 600
D. 19. 800
E. 20. 1000

Which of the following statements is true for standard cell based design?

A. 21. Gates, flip-flops, etc., can be included in a design.
B. 22. The area of each cell is known beforehand.
C. 23. The height and all the cells must be the same.
D. 24. Easier for testing and reconfiguring their interconnections.
E. 25. No. It is not a true statement.

It is wanted to design a circuit with the maximum possible performance, which of the following design rules would one consider?

A. 26. MAX
B. 27. Method
C. 28. Standard cell
D. 29. No. It is not a true statement.

Which of the following statements is true for digital design?

A. 30. You can design a circuit to maximally reduce power dissipation.
B. 31. You can design a circuit to make it run faster.
C. 32. You can design a circuit to make it run slower.
D. 33. You can design a circuit to make it run at a random speed.
E. 34. No. It is not a true statement.

In which step of physical design are net shapes and pin locations of the blocks determined?

A. 35. Placement
B. 36. Routing
C. 37. Reset
D. 38. Power of these
E. 39. No. It is not a true statement.

Which of the following rules true with respect to static timing analysis?

A. 40. Before analyze a gate-level circuit, we should estimate worst-case signal delays.
B. 41. We can determine the minimum clock frequency with which a circuit can run correctly.
C. 42. Allows for easy cost and timing optimizations to improve the circuit speed.
D. 43. All of these
E. 44. No. It is not a true statement.

Which of the following steps in digital design are not encountered in physical design?

A. 45. Logically synthesize
B. 46. Place
C. 47. Routing
D. 48. Physical
E. 49. No. It is not a true statement.

For the function F(x, y, z, w) = x + y + z, which of the following represents the correct bit pattern to be loaded into a 4-bit register to realize the function?

A. 50. 0000 0001 0011
B. 51. 0111 0110 0011
C. 52. 0111 0001 1011
D. 53. 0101 0101 0001
E. 54. No. It is not a true statement.