Assignment 0

The due date for submitting this assignment has passed. No late submissions will be accepted.

Week Assignment 0

Week 5

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Unit 2 - Week 0 Assignment 0

Q1. Which of the following sets of gates is/are functionally complete? 2 marks each
   a. AND, OR
   b. OR, NOT
   c. OR, XOR
   d. NOT, XOR
   e. NOT, XNOR
   f. NOT, OR

   Correct answer(s): a, b, c, d

Q2. What is the minimum number of 2-input NAND gates required to realize a 4-input NAND function?
   2 marks each
   a. 8
   b. 6
   c. 4
   d. 1

   Correct answer(s): a, b

Q3. The number of flip-flops required to implement a 16-bit ripple carry adder is
   2 marks each

Q4. On what factors does the delay of a combinational circuit depend upon?
   2 marks each
   a. The number of paths in the circuit
   b. The number of gates levels
   c. The frequency of the clock
   d. None of the above

   Correct answer(s): a, b, c

Q5. Without using any additional gates, which of the following switching functions can be realized by a 2-to-4 multiplexer?
   2 marks each
   a. NOT
   b. AND
   c. OR
   d. XOR
   e. XNOR

   Correct answer(s): a, b, c

Q6. Consider a 16 Kbyte hard disk memory. How many address lines will be there?
   2 marks each
   a. 10
   b. 16
   c. 18
   d. 24

   Correct answer(s): a

Q7. For a simple NOR gate realization using CMOS technology, the total number of MOS transistors required will be
   2 marks each

   Correct answer(s): a

Q8. For a CMOS gate, the rise time at the output will depend on:
   2 marks each
   a. The effective resistance of the pull-up network
   b. The effective resistance of the pull-down network
   c. The total output load of the output point is driving
   d. All of the above

   Correct answer(s): a, b, c

Q9. For a 4-bit/8-bit RISC, flip-flops store the inputs to the instruction decoder, and load 256 rectangular periodic signals to the clock input. The frequency of the signal generated at the output will be
   2 marks each

   Correct answer(s): a

Q10. Which of the following statements is/are true?
   2 marks each
   a. FIPS 300 based designs take less design effort as compared to ASIC designs.
   b. FIPS 300 based designs are more cost-effective than ASIC implementations.
   c. FIPS 300 based designs can be secured even in high-traffic environments, but this security comes at a cost.
   d. All of the above

   Correct answer(s): a, b, c