Assignment 6

The due date for submitting this assignment has passed. 

1. The minimum number of discrete voltage levels necessary to be present in the system (including 0) to achieve the target consumption can be indicated by
   a. \( V_1 \)
   b. \( V_2 \)
   c. \( V_3 \)
   d. \( V_4 \)
   e. \( V_5 \)
   f. \( V_6 \)

2. Considering a scenario having a finite number of discrete voltage levels to work with, which restricts where to run and which voltage levels are allowed for each task, the following statements are correct:
   a. Operating systems b. Compiler options c. Both a and b d. Compiler options

3. The assignment is to implement a voltage scheduling framework for
   a. Single-precision computing
   b. Double-precision computing
   c. Both single and double precision
   d. None of the above

4. The objective of energy efficiency of platforms is to
   a. Reduce the number of instructions issued
   b. Operate at a lower voltage level
   c. Both a and b
   d. None of the above

5. The top-down approach to implementing an OS is
   a. First, implement the kernel, then the device drivers
   b. First, implement the device drivers, then the kernel
   c. Both a and b
   d. None of the above

6. The switch-level optimization techniques
   a. Visually optimize the code
   b. Verify the optimization using a simulator
   c. Both a and b
   d. None of the above

7. The ARM Architecture allows the execution of
   a. RISC assembly instructions
   b. CISC instructions
   c. Both RISC and CISC instructions
   d. None of the above

8. The microcontroller's on-chip peripheral is
   a. A UART
   b. A CAN bus
   c. Both a and b
   d. None of the above

9. The on-chip peripheral for implementing
   a. UART
   b. CAN bus
   c. Both UART and CAN bus
   d. None of the above

10. The on-chip peripheral for implementing
    a. SPI
    b. I2C
    c. Both SPI and I2C
    d. None of the above