Unit 4 - Week 2: Instruction Pipeline Principles

Assignment 2

Due on 2018-06-21, 23.59 BST.

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1. MIPS Harvard also known as ________
   / point

2. Which of the following statements about the pipelining concept is true?
   / point
   - The instruction fetching stage is always the first stage in a pipeline.
   - The instruction encoding stage is always the second stage in a pipeline.
   - The instruction register stage is always the third stage in a pipeline.

3. Given the following program:
   int main()
   {
       int a = 5;
       int b = 10;
       int c = a + b;
   }
   What is the correct output of this program?
   / point
   - 15
   - 10
   - 5
   - Cannot be determined

4. Which of the following statements about the pipeline concept is true?
   / point
   - The instruction encoding stage is always the second stage in a pipeline.
   - The instruction register stage is always the third stage in a pipeline.
   - The instruction decode stage is always the fourth stage in a pipeline.

5. The execution time of a program is ________
   / point
   - Equal to the sum of the execution times of all instructions
   - Equal to the sum of the execution times of all instructions multiplied by the instruction clock cycle.
   - Equal to the sum of the execution times of all instructions divided by the instruction clock cycle.

6. The instruction fetch stage is ________
   / point
   - The stage where the instruction is loaded into the instruction register.
   - The stage where the instruction is decoded.
   - The stage where the instruction is executed.

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![Image of a computer architecture diagram]

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Notes:

- MIPS: Modified Instruction Pipeline
- Harvard architecture
- Von Neumann architecture