Assignment 1

Due on 2019-09-11, 23:59 IST.

ASSIGNMENT DUE DATE: [Insert Date]

Assignment 1

1. An instruction pipeline was designed with five stages, individually each of the stages takes 2.3, 1.5, 3.1, 3.3, and 3.5 ms, respectively. The pipeline operates with 94% efficiency. What is the maximum number of instructions that can be executed in a single clock cycle of the pipeline?

2. (a) What should be the ideal clock specification for a decoder that is connected to the address bus of a processor that has an addressability of 144 MB of memory? (Assume word length is 1 byte)

3. For a 64x64 ALU to compute the product of two numbers, what is the size of the scalar value that is used to compute the effective address? (Assume that both numbers are of the same size and that the product is a single value)

4. Which of the following is not a 80x86 CPU instruction?

5. Which of the following statements is false with respect to instruction pipelines?

6. A system has 32-bit data paths and 24-bit instruction paths. What is the maximum number of instructions that can be executed in a single clock cycle of the pipeline?

7. The bit-width of the barrel shifter is 32 bits. If the barrel shifter is to be used to implement a 2's complement subtraction, what is the maximum number of instructions that can be executed in a single clock cycle of the pipeline?

8. Given an instruction pipeline operating at 1 GIPS that takes 5 cycles to finish its execution: 30% memory instructions result in stall at 5 cycles. Assume a basic CPI without stalls at 1 and there are 10% memory instructions, the effective CPI is ...

9. A 16x16 multiplier with 80x86 architecture is used in a processor. How many cycles will it take to perform a 16x16 multiplication?

10. A program has 40% multimedia instructions, what is the overall speedup gained while running the program on a processor with the new INRU that it ran on the processor without this INRU?

11. A new multimedia instruction set (MIS) that includes multimedia instructions is added to a processor. How many cycles will it take to perform a 16x16 multiplication?

12. Given an instruction pipeline operating at 1 GIPS that takes 5 cycles to finish its execution: 30% memory instructions result in stall at 5 cycles. Assume a basic CPI without stalls at 1 and there are 10% memory instructions, the effective CPI is ...

Accepted Answers:

[Insert Accepted Answers]

[Insert Footer]

-Swamy

Unit 1 - Week 1: Basic Computer Organization

Course outline

How to access the portal

Week 1: Basic Computer Organization
- Lesson 1: Review of Basic Computer Organization
- Lesson 2: Performance Improvement Techniques
- Lesson 3: Introduction to Instruction Execution
- Lesson 4: Tutorial - Instruction Pipeline Performance

Week 2: Instruction Pipeline

- Lesson 1: Pipeline Scheduling Techniques
- Lesson 2: Superscalar Processing
- Lesson 3: Cache Memory Organizations
- Lesson 4: Primary and Secondary Memory Systems
- Lesson 5: The CPU and Memory Interface

Week 3: Input/Output

- Lesson 1: Input/Output Devices
- Lesson 2: Interfacing Techniques

Unit 2: Processor Architecture

- Lesson 1: Processor Architecture Overview
- Lesson 2: Microarchitecture Principles
- Lesson 3: Advanced Processor Architectures

MNTIL - Advanced Computer Architecture

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