Assignment 2

Due on 2020-03-11, 23:59 EST.

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

1. For a cache with associativity = 2, LRU block replacement is equivalent to
   \[ \text{HRU} \]
   \[ \text{LFU} \]
   \[ \text{FCU} \]
   \[ \text{SRU} \]
   \[ \text{No, the answer is incorrect.} \]
   Accepted Answers:
   \[ \text{SRU} \]

2. Which of the following statements is/are true for fully associative caches?
   \[ \text{[a] Only one position is replaced} \]
   \[ \text{[b] Any position can be replaced} \]
   \[ \text{[c] They have only compulsory misses} \]
   \[ \text{[d] They have only capacity misses} \]
   \[ \text{[e] They have both conflict misses and capacity misses} \]
   \[ \text{[f] They do not have conflict misses.} \]
   \[ \text{No, the answer is incorrect.} \]
   Accepted Answers:
   \[ \text{[a, c]} \]

3. Which of the following types of cache needs a dirty bit in each of its blocks?
   \[ \text{[a] Write-back cache} \]
   \[ \text{[b] Write-through cache} \]
   \[ \text{[c] Invalidation cache} \]
   \[ \text{[d] Last-in-cache cache} \]
   \[ \text{No, the answer is incorrect.} \]
   Accepted Answers:
   \[ \text{[a, c, d]} \]

4. If an address is referenced, then the same address will be referenced again with a high probability. This is called the principle of
   \[ \text{[a] Spatial locality} \]
   \[ \text{[b] Block replacement} \]
   \[ \text{[c] Temporal locality} \]
   \[ \text{[d] Address aliasing} \]
   \[ \text{Accepted Answers:} \]
   \[ \text{Typical locality} \]

5. Which of the following is true for write operation in a write allocate cache?
   \[ \text{[a] The block containing the miss is brought to the cache for writing} \]
   \[ \text{[b] The block is rewritten in the main memory only} \]
   \[ \text{[c] The block is rewritten in the main memory and then immediately bring the modified block to the cache} \]
   \[ \text{[d] The block containing the miss is brought to the cache for writing and then immediately write both the block to the main memory} \]
   \[ \text{No, the answer is incorrect.} \]
   Accepted Answers:
   \[ \text{[a, c]} \]

6. Which of the following is true for write operation in a write-through cache (Assume one level of cache and main memory in the memory hierarchy)?
   \[ \text{[a] The data update in the cache memory results in immediate update in the main memory} \]
   \[ \text{[b] The data is never written to the main memory} \]
   \[ \text{[c] The data is written to the main memory only when a dirty cache block is evicted} \]
   \[ \text{[d] The data is written to the main memory only when an unused cache block is evicted} \]
   \[ \text{No, the answer is incorrect.} \]
   Accepted Answers:
   \[ \text{[a, c]} \]

7. A 1 MB cache of a block size of 32 bytes has an associativity of 8. The system is using 32-bit physical address. Which set of this cache will be indexed to know whether the physical address 0x01234567 is a cache hit or not? (Give Set numbers from 0, 1, 2, ...)