Unit 3 - Week 1: Course Introduction & Pipelined Instruction Execution Principles

Assignment 1

The due date for submitting this assignment has passed.

Due on 2020-03-04, 23:59 IST.

1. An instruction decoder within a microprocessor input clock cycle to output the binary value of the instruction. Which of the following is the best possible value for an instruction?
   - 5
   - 10
   - 15
   - 20

   Accepted Answers:
   - 15

2. Which stage is in a 6 stage RISC MIPS instruction pipeline reads the contents of register file?
   - ID
   - EX
   - MEM
   - WI

   Accepted Answers:
   - EX

3. An instruction pipeline was designed with four stages, individually each of the stage take 2, 2.5, 2.5, and 2.5 clock cycles, respectively, for completion of the operations. The pipeline stall latency is 3.25 clock cycles. What is the minimum cycle time of the pipeline?
   - 3.25
   - 4.75
   - 5.25
   - 6.75

   Accepted Answers:
   - 5.25

4. Which of the following is the operation performed in the MMU stage for a LOAD instruction is a 6-stage RISC instruction pipeline?
   - Translate the address from the ALU to the memory location.
   - Load address of the destination location from memory to ALU.
   - Load the contents of the memory location whose address is computed in EX stage.
   - Load MMU pipeline register.

   Accepted Answers:
   - Load MMU pipeline register.

5. Which of the following cannot be a valid instruction for a stock processor? Hint: B, C, and D is a address of a memory location and F is the name of a register.
   - ADD R, A, B
   - SUB R, A, B
   - MUL R, A, C

   Accepted Answers:
   - ADD R, A, B

6. If a 32-bit value (0110100101000111100111001101001) is stored in memory addresses 1202, 1201, 1200, and 1203 in big endian format, then the location 1202 holds the value?
   - 0x03
   - 0x02
   - 0x01
   - 0x00

   Accepted Answers:
   - 0x02

7. When an instruction pipeline fetches and executes more than one instruction per clock cycle then it is called-----.
   - simple pipeline
   - superscalar pipeline
   - multithreaded pipeline
   - multithreaded pipeline

   Accepted Answers:
   - superscalar pipeline

8. A 64-bit microprocessor has a branch instruction that supports conditional executing. How many states in clock cycles will be there between a part of adjacent MUL instructions that have a HW dependency between them?

   Accepted Answers:
   - Type: Integer
   - Value: 3

9. A program which has 600 instructions has 90% branch instructions, 90% load/store instructions and the rest are ALU instructions. The program is running on a processor operating at 3 clocks. The CPI of branch, load/store and ALU instructions are 3, 1, and 1, respectively. What is the average time that a program takes in seconds (correct to 2 decimal places)?

   Accepted Answers:
   - Type: Integer
   - Value: 12.50

10. The average branch unit speed up branch instructions by 5 times. In an application one third of the instructions are branch instructions. What is the overall speed up correct to two decimal places?

   Accepted Answers:
   - Type: Integer
   - Value: 1.67