Assignment-10

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment. Due on 2018-10-10, 23:59 IST.

1) The components of Scalable Core Test Architecture are:

- Test Access Mechanism
- Wrapper
- Source and Sink for test stimuli and responses
- All of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
All of the above

2) Which of the following is FALSE about TAM?

- Transports test responses from the CUT to the test sink.
- Wider TAM, more I/Os are required.
- Loads and executes test instructions.
- Delivers test stimuli from the test source to the CUT.

No, the answer is incorrect.
Score: 0
Accepted Answers:
Loads and executes test instructions.

3) Which of the following are the valid operating modes of IEEE P 1500 standard?

- INTEST
- XTEST

No, the answer is incorrect.
Score: 0
Accepted Answers:

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4) Which of the following is **FALSE** about the WIR circuitry of the P1500 Wrapper architecture?

- Loads and executes test instructions
- Configures the operation of the wrapper
- Consists of boundary scan cells (BSCs)
- Decodes loaded instructions

No, the answer is incorrect.
Score: 0

Accepted Answers:
Consists of boundary scan cells (BSCs)

5) The state transition diagram shown in the below figure corresponds to which fault in a memory?

- Stuck at one in a memory cell
- Stuck at zero in a memory cell
- Up transition fault in a memory cell
- Down transition fault in a memory cell

No, the answer is incorrect.
Score: 0

Accepted Answers:
Up transition fault in a memory cell

6) The state transition diagram shown in the below figure corresponds to which fault in a memory?

- Stuck at zero in a memory cell
- Stuck at one in a memory cell
- Down transition fault in a memory cell
- Up transition fault in a memory cell

No, the answer is incorrect.
Score: 0
7) From the context of memory testing, the types of faults considered in address decoder are: 1 point

- No address can access a certain cell
- With a particular address, multiple cells are simultaneously accessed
- A particular cell can be accessed with multiple addresses
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
All of the above

8) March Test is most appropriate for? 1 point

- Testing Combinational circuits
- Testing memory
- Testing Sequential circuits
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Testing memory

9) The bridging faults <0,0|0,0>,<0,1|1,1>,<1,0|1,1>,<1,1|1,1> are? 1 point

- AND Bridging faults
- OR Bridging faults
- Both b & c
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
OR Bridging faults