Assignment for Week 10

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment. Due on 2019-04-10, 23:59 IST.

1) In internal fragmentation, memory is internal to a partition and:

- is being used
- is not being used
- is always used
- None of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
is not being used

2) Consider a system with 32-bit virtual address space. What will be the number of page table entries if the page size is 1KB?

- 232
- 222
- 210
- 242

No, the answer is incorrect.
Score: 0
Accepted Answers:
222

3) Larger page sizes leads to 1 point

- Transfer errors
- Increase in operation time

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4) Which among the following is true?  
- The memory allocated to each page is contiguous.  
- The offset is different in a virtual address and a physical address  
- Logical address space can be smaller than physical address space  
- Segmentation avoids external memory fragmentation

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
The memory allocated to each page is contiguous.

5) Assume that the virtual address space of system is $2^{64}$ bits and physical memory is 64KB. 1 point  
If the size of the page is 1KB and page table entry size is 2Bytes, what is the size of inverted page table?  
- 252 Bytes  
- 251 Bytes  
- 64 Bytes  
- 128 Bytes

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
128 Bytes

6) Which among the following will be triggered when a request to the page that is not present in the main memory is accessed?  
- Interrupt  
- Request  
- Page fault  
- None of the above

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
Page fault

7) A CPU generates 32-bit virtual addresses. The page size is 4KB. The processor has a TLB 1 point which can hold 128 entries and is 4-way set associative. The size of the TLB tag is?  
- 15  
- 11  
- 12  
- 14

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
15

8) Page fault occurs when  
- 1 point
9) TLB lookup takes 5ns and memory access time is 100ns in a hypothetical system. If the TLB hit ratio is 80%, what will be the effective access time assuming that the system is cache-less?

- 100ns
- 120ns
- 105ns
- 125ns

No, the answer is incorrect.
Score: 0
Accepted Answers:
- a requested page is not in memory

10) Consider a paged system with page table stored in virtual memory with virtual address space size of $2^{64}$ bits. If a memory access takes 128ns, how long does a paged memory reference take?

- 128ns
- 120ns
- 256ns
- 64ns

No, the answer is incorrect.
Score: 0
Accepted Answers:
- 256ns