Assignment for Week 0

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment.

1) The Binary representation of decimal number 485 is

- 111100101
- 111110111
- 101111111
- 101110111

No, the answer is incorrect.
Score: 0
Accepted Answers:
111100101

2) One byte equals to how many bits?

- 4
- 8
- 12
- 16

No, the answer is incorrect.
Score: 0
Accepted Answers:
8

3) In which of the following gates, the output is 1, if and only if at least one input is 1?

- NOR
- AND
- OR

1 point
4) What is the minimum number of two-input NAND gates used to perform the function of two input OR gate?

- 1
- 2
- 3
- 4

No, the answer is incorrect.
Score: 0
Accepted Answers: 3

5) How many inputs and outputs does a JK flip-flop have (excluding the clock)?

- 2 inputs and 2 outputs
- 1 input and 2 outputs
- 1 input and 1 output
- None of the above

No, the answer is incorrect.
Score: 0
Accepted Answers: 2 inputs and 2 outputs

6) The number of cells in a 3-variable K-map is

- 12
- 32
- 8
- 16

No, the answer is incorrect.
Score: 0
Accepted Answers: 8

7) The number of full and half-adders required to add 16-bit numbers is

- 8 half-adders, 8 full-adders
- 1 half-adder, 15 full-adders
- 16 half-adders, 0 full-adders
- 4 half-adders, 12 full-adders

No, the answer is incorrect.
Score: 0
Accepted Answers: 1 half-adder, 15 full-adders

8) Which of the following expression follows DeMorgan’s theorem?

- \((A \cdot B)' = A' + B'\)
- \((A + B)' = A' \cdot B\)
- \(A' + B' = A' \cdot B'\)
- None of the above.

No, the answer is incorrect.
9) Assume that AND, OR and NOT gates are used in the construction of the multiplexer. How many NOT gates (minimum) are required for the construction of a 8-to-1 multiplexer? 

- 5
- 4
- 2
- 3

No, the answer is incorrect.

10) The logical addresses generated by the CPU are mapped onto physical memory by ____.

- Relocation register
- TLB
- MMU
- None of the above

No, the answer is incorrect.

11) A clock with frequency X (MHZ) is applied to a cascaded counter containing a modulus-4 counter, a modulus-8 counter, and a modulus-10 counter. The lowest output frequency possible is ________

- X/4 MHz
- X/8 MHz
- X/32 MHz
- X/320 MHz

No, the answer is incorrect.

12) Which of the following describes most appropriately a “shift register”? 

- The register that can shift information bits to another register
- The register that can shift information bits either to the right or to the left
- The register that can shift information bits to the right only
- The register that can shift information bits to the left only

No, the answer is incorrect.