Assignment 12

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment.

Due on 2019-10-23, 23:56 IST.

1) The tree covering algorithm in technology mapping could require an execution time (excluding the time required for matching) that is Polynomial in the sizes of the pattern and subject graphs

   - TRUE
   - FALSE

No, the answer is incorrect. Score: 0
Accepted Answers: TRUE

2) In FPGA synthesis, the matching part of technology mapping is likely to be more complex than in ASIC synthesis

   - TRUE
   - FALSE

No, the answer is incorrect. Score: 0
Accepted Answers: FALSE

3) Static timing analysis requires the use of test patterns to estimate the clock period

   - TRUE
   - FALSE

No, the answer is incorrect. Score: 0
Accepted Answers: FALSE

4) The controlling input value of an OR gate and an AND gate are, respectively:

   - 1, 1
   - 0, 0
   - 1, 0
   - 0, 1

No, the answer is incorrect. Score: 0
Accepted Answers: 1, 0

5) In timing analysis, a positive slack indicates sensitivity of a circuit to a signal in what way?

   - The signal can be delayed without affecting the critical path
   - The signal is on the critical path
   - The signal will not meet timing requirements
   - Gates connected to this signal need to be made faster

No, the answer is incorrect. Score: 0
Accepted Answers: The signal can be delayed without affecting the critical path

6) If it is not possible to sensitize a path in a netlist, then it is a False Path

   - TRUE
   - FALSE

No, the answer is incorrect. Score: 0
Accepted Answers: FALSE

7) A cell library used by Technology Mapping is likely to contain what kind of information regarding the cell?

   - Area
   - Delay
   - Power
   - Fanout

No, the answer is incorrect. Score: 0
Accepted Answers: Area

8) Which of the following conditions are true when an event propagates along a path in a netlist?

   - The boolean difference of the output with respect to the input is 0 for all nodes along the path
   - The boolean difference of the input with respect to the output is 0 for all nodes along the path
   - The boolean difference of the output with respect to the input is 1 for all nodes along the path
   - The boolean difference of the input with respect to the output is 1 for all nodes along the path

No, the answer is incorrect. Score: 0
Accepted Answers: The boolean difference of the output with respect to the input is 1 for all nodes along the path