Unit 11 - Week 9

Assignment 9

The due date for submitting this assignment has passed. 
As per our records you have not submitted this assignment.

1) If two transitions from states S0 and S1 have a common next state S2 in an FSM, then:
   - It is worth assigning close codes to S0 and S2.
   - It is worth assigning close codes to S1 and S2.
   - It is worth assigning close codes to S0 and S1.
   - It is not worth assigning close codes to any pair of these states

No, the answer is incorrect.
Score: 0
Accepted Answers:
- TRUE

2) If two transitions from states S0 and S1 have a common next state S2 in an FSM, then it is worth assigning close codes to S0 and S1.

No, the answer is incorrect.
Score: 0
Accepted Answers:
- TRUE

3) If two transitions from states S0 and S1 have a common next state S2 in an FSM, then which of the following is the best ordering?

- S0 (**1000**), S1 (**1100**), S2 (**0000**)
- S0 (**1000**), S1 (**1100**), S2 (**0000**)
- S0 (**1000**), S1 (**1100**), S2 (**1000**)
- S0 (**1000**), S1 (**1111**), S2 (**0000**)

No, the answer is incorrect.
Score: 0
Accepted Answers:
- S0 (**1000**), S1 (**1100**), S2 (**0000**)

4) In the heuristic proposed for the Graph Embedding problem, higher priority is given to the encoding states with higher numbers of skipping transitions:
   - TRUE
   - FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
- FALSE

5) Refining an individual gate (node) can result in:

   - Increased area
   - Decreased area
   - Increased clock period requirement
   - Decreased clock period requirement

No, the answer is incorrect.
Score: 0
Accepted Answers:
- Increased area

6) In the graph representation of a sequential circuit for retiming optimization, which of the following are true?

   - The nodes represent the combinational logic gates.
   - The nodes represent the registers.
   - The edge weights represent the total delay of the combinational gates in a path.
   - The edge weights represent the number of register stages in a path.

No, the answer is incorrect.
Score: 0
Accepted Answers:
- The nodes represent the combinational logic gates.

7) In the graph representation used in the retiming problem, edge weights may become negative after the legal retiming of a node/gate.

   - TRUE
   - FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
- TRUE

8) In the graph representation used in the retiming problem, some path delays may be affected by the retiming of a node/gate.

   - TRUE
   - FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
- TRUE

9) In the graph representation used in the retiming problem, some path weights may be affected by the retiming of a node/gate.

   - TRUE
   - FALSE

No, the answer is incorrect.
Score: 0
Accepted Answers:
- TRUE

10) For sequential circuits, what happens during the retiming optimization that reduces the overall execution time?

   - Latency (number of cycles) gets reduced
   - Cycle time (required clock period) gets reduced
   - Both latency and cycle time gets reduced
   - Neither latency nor the cycle time is reduced

No, the answer is incorrect.
Score: 0
Accepted Answers:
- Cycle time (required clock period) gets reduced