Assignment 6

The last day for submitting this assignment is passed. As per our records you have not submitted this assignment.

Due on 2019-09-11, 23:59 IST.

1. The loop unrolling transformation exposes parallelism in the specification under what conditions? (1 point)
   - When the number of iterations is small
   - When there are serial loops
   - When there are independent operations across the iterations
   - When there are memory accesses across the loop body
   - No, the answer is incorrect.
   - Correct Answer: 3
   - When there are independent operations across the iterations

2. Assume that the size of a loop requires 18 clock cycles when scheduled, and the loop goes through 8 iterations. Which of the following could be the final final schedule length of the fully unrolled code?
   - 180
   - 360
   - 720
   - 90
   - No, the answer is incorrect.
   - Correct Answer: 720
   - 90

3. The memory access delay increases if we increase the number of read ports of a memory, keeping the capacity the same. (1 point)
   - TRUE
   - FALSE
   - No, the answer is incorrect.
   - Correct Answer: FALSE
   - No, the answer is incorrect.

4. The schedule length of a DSP can vary if we increase the number of read ports of a memory, keeping the capacity the same. (1 point)
   - TRUE
   - FALSE
   - No, the answer is incorrect.
   - Correct Answer: FALSE
   - No, the answer is incorrect.

5. Which of the following is NOT TRUE when the function merging transformation is applied to a specification? Assume that the FSM's combinatorial logic's delay is not considered.
   - It may decrease the size of the sequential representation.
   - It may increase the size of the sequential representation.
   - It may lead to shorter schedules.
   - It may lead to longer schedules.
   - No, the answer is incorrect.
   - Correct Answer: It may decrease the size of the sequential representation.
   - It may increase the size of the sequential representation.
   - It may lead to shorter schedules.
   - It may lead to longer schedules.

6. Consider two synthesis solutions (A) All amps are shared in a single memory module (B) All amps are shared in different memory modules.
   - A leads to smaller area.
   - B leads to shorter schedule lengths.
   - B leads to shorter schedule lengths.
   - A leads to shorter schedule lengths.
   - No, the answer is incorrect.
   - Correct Answer: A leads to shorter schedule lengths.
   - B leads to shorter schedule lengths.

7. The Tree height Reduction transformation always leads to improved performance. (1 point)
   - TRUE
   - FALSE
   - No, the answer is incorrect.
   - Correct Answer: FALSE
   - No, the answer is incorrect.

8. The Control Flow to Data flow transformation primarily targets:
   - Arithmetic constructs
   - Conditional constructs
   - Bit-wise operators
   - Function calls
   - No, the answer is incorrect.
   - Correct Answer: Conditional constructs
   - Bit-wise operators

9. The scheduling step in high level synthesis results when operations are being mapped to specific clock cycles. (1 point)
   - TRUE
   - FALSE
   - No, the answer is incorrect.
   - Correct Answer: FALSE
   - No, the answer is incorrect.

10. In resource-constrained scheduling,
    - A deadline constraint is given, and the scheduler has to ensure resources to complete the tasks before the deadline.
    - Resources are fixed and the scheduler has to minimize the number of clock cycles.
    - Resources are assumed to be infinite, and the scheduler tries to eliminate the number of clock cycles.
    - A deadline constraint is given and the scheduler tries to minimize the number of clock cycles.
    - No, the answer is incorrect.
    - Correct Answer: A deadline constraint is given and the scheduler tries to minimize the number of clock cycles.
    - Resources are fixed and the scheduler has to minimize the number of clock cycles.

11. When assignments of a variable occur in jmp but not at branches of a conditional construct, it can result in inferences of a
    - Jump
    - Complex conditional circuit
    - Loops
    - Decoder
    - No, the answer is incorrect.
    - Correct Answer: Jump
    - Complex conditional circuit

12. Aggressive loop unrolling might blow up the number of states in the control FSM generated during synthesis. (1 point)
    - TRUE
    - FALSE
    - No, the answer is incorrect.
    - Correct Answer: FALSE
    - No, the answer is incorrect.