Assignment 4

Due on 2016-08-23, 23:59 IST.

1. Which of the following is an OUTPUT of the High-level Synthesis process? 1 point
   - HLS description
   - Component Library
   - Post-Design netlist
   - High-level description
   Accepted Answers: HLS description
   Score: 1

2. Which of the following are true regarding the F2RM and D2D2AR in High-level Synthesis? 1 point
   - Control signals are sent by the D2D2AR to the F2RM
   - Commit signals are sent by the D2RM to the D2D2AR
   - Status signals are sent by the F2RM to the D2D2AR
   - Status signals are sent by the D2D2AR to the F2RM
   Accepted Answers: Status signals are sent by the D2D2AR to the F2RM
   Score: 1

3. The resource library that is an input to the HLS process could contain what information? 1 point
   - Scheduling algorithm
   - Component views
   - Register allocation algorithm
   - Component delay
   Accepted Answers: Component delay
   Score: 1

4. If the control of an operation produces in one clock pulse a value different from the one before, which one of the following is inferred? 1 point
   - A multiplexer
   - A register
   - A latch
   - A decoder
   Accepted Answers: A register
   Score: 1

5. Sharing of an adder by two different operations ALWAYS leads to the inference of a multiplexer at its input. 1 point
   - TRUE
   - FALSE
   Accepted Answers: FALSE
   Score: 1

6. The number of registers inferred when a DFS is subject to HLS is less than or equal to the number of DFS edges belonging to clock cycle boundaries. 1 point
   - TRUE
   - FALSE
   Accepted Answers: TRUE
   Score: 1

7. Penrose curve consists of all solution points that are: 1 point
   - The set of feasible solutions
   - The set of infeasible solutions
   - Not superior to any other point in the design space
   - Not inferior to any other point in the design space
   Accepted Answers: Not superior to any other point in the design space
   Score: 1

8. The output of the kernel analysis phase consists of a stream of tokens. 1 point
   - TRUE
   - FALSE
   Accepted Answers: FALSE
   Score: 1

9. Verifying the presigner of the specification is the job of the Prover. 1 point
   - TRUE
   - FALSE
   Accepted Answers: TRUE
   Score: 1

10. The abstract syntax tree is usually created at the end of parsing a specification. 1 point
    - TRUE
    - FALSE
    Accepted Answers: FALSE
    Score: 1

11. Which of the following is NOT a valid information captured within resource-library used in HLS? 1 point
    - Area of each component
    - Functionality of each component
    - Connections between different library components
    - Delay of each component
    Accepted Answers: Connections between different library components
    Score: 1

12. In high-level synthesis, "type" mismatches in signal assignments present in the behavioral specification are checked during semantic checking. 1 point
    - TRUE
    - FALSE
    Accepted Answers: TRUE
    Score: 1