Assignment 3

The deadline for submitting this assignment has passed.
As per your records you have not submitted this assignment.

1. A simple 2-input AND gate can be modelled in VHDL, with a process that monitors sensitivity list with assert statement:
   - TRUE
   - FALSE
   Accepted Answers: TRUE

2. The above process is incorrect.
   - TRUE
   - FALSE
   Accepted Answers: FALSE

A VHDL process having the statement “A = B & C” within a always triggered whenever either A or B changes irrespective of C and B are signals:
- TRUE
- FALSE

No, the process is incorrect.

3. A process triggered with an assert statement within a process executing
   - TRUE
   - FALSE
   Accepted Answers: FALSE

A VHDL statement of VHDL can occur within a loop:
- TRUE
- FALSE

No, the answer is incorrect.

4. B always statement of a process can occur within a branch of an if statement:
- TRUE
- FALSE

No, the answer is incorrect.

5. One way of modelling combinational logic in a VHDL process is to place all the input signals in the sensitivity list:
- TRUE
- FALSE

No, the answer is incorrect.

6. What does the following VHDL statement represent? “(test until ‘1’ and ‘1’)”
- An unconditional halt
- Square root of X
- Change in value of signal X
- A logic value of signal X

No, the answer is incorrect.

7. The purpose of a VHDL testbenches could include which of the following applications?
- To provide inputs to the design under test
- To observe outputs from the design under test
- To specify constraints for simulation
- To report timing relations during simulation

No, the answer is incorrect.

8. A testbench is executed:
- A logic value of signal X
- A logic value of signal X

No, the answer is incorrect.

9. Which of the following are realistic connections involving VHDL testbenches?
- Output ports of the testbenches are connected to the input ports of the design under test
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- Input ports of the testbenches are connected to the input ports of the design under test

No, the answer is incorrect.

10. Generic parameters can be used in VHDL to parameterize:
- Signals in assigned parameters
- Names of ports
- Names of entities
- Names of packages

No, the answer is incorrect.

11. VHDL processes can be nested (a process inside another process):
- TRUE
- FALSE

No, the answer is incorrect.

12. VHDL signals are declared either within processes or within architectures:
- TRUE
- FALSE

No, the answer is incorrect.

13. In VHDL, the architecture to use for a specific entity can be specified using:
- GENERIC
- ENTITY
- ARCHITECTURE
- ATTRIBUTE

No, the answer is incorrect.

14. Configuration statement:
- entity
- architecture
- entity
- configuration

No, the answer is incorrect.

15. Configuration statement:
- entity
- architecture
- entity
- configuration

No, the answer is incorrect.