Assignment 2

The due date for submitting this assignment has passed.

As per our records you have not submitted this assignment.

1) The functionality of a VHDL model is captured in its Architecture.
   - True
   - False
   - No, the answer is incorrect.
   - Score: 0
   - Accepted Answers: True

2) The results of a VHDL simulation are unaffected by changes in the order of specification of concurrent signal assignments.
   - True
   - False
   - No, the answer is incorrect.
   - Score: 0
   - Accepted Answers: True

3) When is a VHDL signal assignment executed?
   - When any signal changes on the left hand side or right hand side of the assignment
   - When any signal changes on the left hand side of the assignment
   - When any signal changes on the right hand side of the assignment
   - Upon every rising edge of a clock signal
   - No, the answer is incorrect.
   - Score: 0
   - Accepted Answers: When any signal changes on the right hand side of the assignment

4) If a signal B appears twice on the right hand side of a signal assignment statement (with signal A on the left hand side), the statement is executed twice when B changes.
   - True
   - False
   - No, the answer is incorrect.
   - Score: 0
   - Accepted Answers: False

5) Spikes at the input to a VHDL model are suppressed in the transport delay mechanism.
   - True
   - False
   - No, the answer is incorrect.
   - Score: 0
   - Accepted Answers: False

6) Which of the following are true?
   - A transaction corresponds to a change in value of a signal, but an event need not correspond to a change
   - An event corresponds to a change in value of a signal, but a transaction need not correspond to a change
   - Both transactions and events correspond to changes in the value of a signal
   - Neither transactions nor events correspond to changes in the value of a signal
   - No, the answer is incorrect.
   - Score: 0
   - Accepted Answers: An event corresponds to a change in value of a signal, but a transaction need not correspond to a change