Assignment 1

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment.

Due on 2019-08-14, 23:59 IST.

1. In a Behavioural Level specification the decision of which operation to perform in which clock cycle has not been taken yet

   TRUE
   FALSE

   Accepted Answer: FALSE

2. In a Behavioural specification the external interface of a design is not indicated

   TRUE
   FALSE

   Accepted Answer: FALSE

3. What is an essential difference between the Chip design and software design flows?

   The chip design flow starts with a high level specification
   The chip design flow is subject to manufacturing errors
   The chip design flow is highly automated
   Formal verification is applicable to the chip design flow

   Accepted Answer: The chip design flow starts with a high level specification

4. Design verification could be performed by checking equivalence between

   Behavioral and RTL level specifications
   HDL and gate level specifications
   State and circuit level specifications
   Gate level specification and transistor level implementation

   Accepted Answer: Behavioral and RTL level specifications

5. Which of the following is lowest in level of abstraction?

   - Adder
   - Multiplexer
   - Memory
   - AND gate

   Accepted Answer: AND gate

6. Which of the following are true about the external interface of a simple memory model?

   - Address is a computational input
   - Address is an optional input
   - Address is a computational output
   - Address is an optional output

   Accepted Answer: Address is a computational input

7. A subset consists of what elements?

   - Component instantiations
   - Interconnections
   - Behavioral constructs
   - Assignment statements

   Accepted Answer: Component instantiations

8. Automation is essential in the synthesis process for what reason?

   - The process can be applied to large specifications
   - A single cell needs to be replaced a large number of times
   - The hardware can be generated fast
   - Computer in high-end processors needs to proceed at very high speed

   Accepted Answer: The process can be applied to large specifications

9. When a netlist has a large number of gates, in what order are the components activated in the real hardware?

   - In increasing order of their sizes
   - In decreasing order of their sizes
   - In parallel
   - In increasing order of their fanout

   Accepted Answer: In parallel

10. Which of the following steps belong to the "Design" stage of the Chip design flow?

    - Specification
    - Sizing of a clock
    - Simulation
    - Synthesis

    Accepted Answer: Specification, Simulation, Synthesis

   Accepted Answer: In parallel