Assignment 4

The due date for submitting this assignment has passed.

As per our records you have not submitted this assignment.

1) Write the following as a memory variable:

   a. Segmented
   b. Linear
   c. Non-Linear
   d. None of the above

   No, the answer is incorrect. Score: 0.

   Accepted Answer: Segmented

2) Write the following as floating point registers:

   a. 0
   b. 16
   c. 10
   d. None of the above

   No, the answer is incorrect. Score: 0.

   Accepted Answer: None of the above

3) Which of the following is not a branch instruction in the ARM ISA:

   a. JR
   b. BEQ
   c. BNE
   d. None of the above

   No, the answer is incorrect. Score: 0.

   Accepted Answer: None of the above

4) The effective address (EAX) of the instruction `LDR R0, =12345678` is ________

   a. 10
   b. 12345678
   c. 10 + 12345678
   d. None of the above

   No, the answer is incorrect. Score: 0.

   Accepted Answer: 10 + 12345678

5) Which of the following is an addressing mode in the 680x0 ISA:

   a. Base-offer
   b. Indexed-index
   c. Register-indexed
   d. None of the above

   No, the answer is incorrect. Score: 0.

   Accepted Answer: None of the above

6) Select the incorrect statement:

   a. The `ldr` instruction takes a base register and a set of registers as arguments
   b. The `ldr` instruction branches to, i.e., it has a target that sets a condition
   c. The instruction results in unconditional jump
   d. None of the above

   No, the answer is incorrect. Score: 0.

   Accepted Answer: None of the above

7) Which of the following is not an ISA:

   a. CRC
   b. CRC
   c. None of the above
   d. Can't say

   No, the answer is incorrect. Score: 0.

   Accepted Answer: CRC

8) In ARM, the program counter is known as ________

   a. Instruction pointer
   b. Address pointer
   c. Stack pointer
   d. Register pointer

   No, the answer is incorrect. Score: 0.

   Accepted Answer: Instruction pointer

9) Select the addressing mode used in the given instruction (for the ARM ISA):

   a. Base-index
   b. Base-index register
   c. None of the above

   No, the answer is incorrect. Score: 0.

   Accepted Answer: Base-index register

10) Memory operand (base + offset) corresponds to the ________ addressing mode:

    a. register-indirect
    b. base-evaluated index register
    c. base-evaluated index
    d. None of the above

    No, the answer is incorrect. Score: 0.

    Accepted Answer: Base-evaluated index