Assignment 12

The due date for submitting this assignment has passed. As per your records you have not submitted this assignment.

Assignment Marks

Week 1: 1 point
- L1, H/T time = L1, Miss rate

Week 2: 0 points
- L1, H/T time = L1, Miss rate * L2, Miss rate

Week 3: 0 points
- L1, H/T time = L1, Miss rate * L2, Miss rate

Week 4: 0 points
- L1, H/T time = L1, Miss rate

Week 5: 0 points
- L1, H/T time = L1, Miss rate

Week 6: 0 points
- A fully associative cache and a direct mapped cache differ in terms of:
  - Presence/absence of a tag array
  - Presence/absence of read bits
  - Presence/absence of write bits
  - None of the above

Week 7: 0 points
- No, the answer is incorrect.

Week 8: 0 points
- No, the answer is incorrect.

Week 9: 0 points
- No, the answer is incorrect.

Week 10: 0 points
- No, the answer is incorrect.

Week 11: 0 points
- No, the answer is incorrect.

Week 12: 0 points
- No, the answer is incorrect.

The Memory Systems Part I

The Memory Systems Part II

The Memory Systems Part II IV

Quiz: Assignment 12

Week 12 Feedback Form

Text Transparencies

Download Videos

Assignment 12

The due date for submitting this assignment has passed. As per your records you have not submitted this assignment.

1) The average memory access time (AMAT) for a hierarchical memory is given as:

- L1, H/T time + L1, Miss rate
- L1, H/T time + L1, Miss rate * L2, Miss rate
- L1, H/T time + L1, Miss rate * L2, Miss rate
- Both c and d

So, the answer is incorrect.

2) A fully associative cache and a direct mapped cache differ in terms of:

- Presence/absence of a tag array
- Presence/absence of read bits
- Presence/absence of write bits
- None of the above

So, the answer is incorrect.

3) The spatial aspect of the locality of reference refers to:

- That an instruction in close proximity of the current instruction will not be executed in the near future
- That the current instruction will not be executed in the near future
- That the current instruction will also be executed at a later point of time
- That an instruction in close proximity of the current instruction will be executed in the near future

So, the answer is incorrect.

4) Which of the following is correct for conflict misses:

- Conflict misses happen when we read data for the first time.
- Conflict misses occur due to the limited size of the cache.
- Conflict misses occur due to the limited amount of associativity in a set associative or direct mapped cache.
- None of the above.

So, the answer is incorrect.

5) A way in a set associative cache is defined as:

- Each entry in a set
- Each entry in a block
- Each entry in a tag array
- None of the above

So, the answer is incorrect.

6) In the write-back cache policy:

- Whenever a write is performed in the cache, the data is also performed to its lower level.
- The write is only performed to its lower level.
- None of the above.

So, the answer is incorrect.

7) The physical memory is broken into fixed-size blocks called:

- Frames
- Pages
- Braving down
- None of the above

So, the answer is incorrect.

8) Hard disk contains a dedicated area to save the names that do not fit in the main memory. This area is known as the:

- Temporary space
- Buffer space
- Swap space
- None of the above

So, the answer is incorrect.

9) The Translation Lookaside Buffer (TLB) is:

- Fully associative cache with a low miss rate
- Fully associative cache with a high miss rate
- Set associative cache with a low miss rate
- Set associative cache with a high miss rate

So, the answer is incorrect.

10) The ideal penalty in terms of the AMAT is defined as (give the most accurate answer):

- AMAT = 1
- AMAT = 1, H/T time
- AMAT = 1, H/T time
- None of these

So, the answer is incorrect.

Due on 2020-04-22, 23:59 HKT.